



TAMPERE UNIVERSITY OF TECHNOLOGY
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NoC benchmarking activities at Tampere University of Technology

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Although benchmarking has a long history in microprocessor and CAD tool design, it has just recently gained attention in network-on-chip (NoC) research. NoC Benchmarking Workgroup (NoCBW) is a collaboration of universities aiming to provide a set of characteristic benchmark designs that help the development and deployment of the NoC paradigm. Such set allows comparison between NoC proposals, which is not possible when proprietary, non-documented test cases are utilized. This enhances the scientific credibility as the new claims and solutions are more easily reproduced and justified by other researchers. At the same time, common guidelines for performance and cost evaluation methodologies are needed.

We at Digital and Computer Systems (DCS) Laboratory of Tampere University of Technology (TUT) have worked on topics regarding the on-chip interconnections for several years. Several network topologies (bus, crossbar, tree, and mesh among others) have been studied both theoretically and in prototypes. Our research team has worked on versatile Transaction Generator tool that is used for on-chip network evaluation and testing. The network traffic is generated according to a process network that defines the transfer sizes and the dependencies. The computation is modeled only by the required number of basic operations. An arbitrary number of processes can be mapped on one processing element (PE). We have already developed an automated tools for creating the profile from given software code. Creating the traffic profile on per-process basis enables evaluating different mapping possibilities in addition to network parameters. In contrast, a traditional per-PE traffic profile is simpler as it does not consider dependencies but it allows only network exploration. However, we believe that both types of application models have a great value in NoC benchmark set. In addition to previous, application (kernels) will play an important role since they allow describing functionality that is more complex. They will be most likely executed in *host-compiled* fashion to avoid using specific instruction set simulators. In host-compilation, the codes are compiled and executed on the workstation and the important events (reads and writes to memory/network) are communicated to network simulator. The execution time is modeled by annotating appropriate delays for code blocks.

Advanced FPGA technology has recently enabled rapid, cost-effective single-chip multiprocessor design and prototyping. It allows executing actual applications in real-time with cost of reduced visibility compared to simulation. Full synthesis, placement, and routing phases are naturally required and, therefore, the evaluation of conceptual methods must be done with simulators. According to our experience, FPGA-prototyping with real software is a crucial step. First, to ensure the correctness and second, to take into account all the subtle effects, such as cache misses, busy wait penalties and interrupt latencies. Otherwise, the results obtained from simple simulations might be too optimistic. For example, the full potential of a network may be impossible to achieve in reality unless all the parts (application code, custom logic, memory hierarchy etc.) are carefully selected and optimized. Currently, we have a working a 16-PE multiprocessor system on a single FPGA running at 100MHz. The results with data-parallel MPEG-4 video encoding are very promising and, to our knowledge, state-of-the-art. The work is in progress to measure the performance with various network topologies.

Further information:

DACI research group: http://www.tkt.cs.tut.fi/research/daci/daci_overview.html

NoCBW: <http://www.ocpip.org/wiki/university/FrontPage>