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First Silicon Solutions Introduces System Navigator Pro™ Series of High Performance Trace Probes

Next-Generation Hardware Platform Addresses SoC Debug and System-Level Verification

PORTLAND, OR, January 30, 2007 -- First Silicon Solutions (FS2), a division of MIPS Technologies, Inc. (NASDAQ: MIPS), today announced the production release of System Navigator Pro™, a high performance high capacity trace probe family designed to address complex SoC debug and system-level verification.

The System Navigator Pro series is FS2's next-generation hardware platform that will enable the deployment of system-level debug solutions that include processor and bus activity as well as system-level performance data. Unlike trace and debug probes available today, the System Navigator Pro solution is the functional equivalent of an integrated high performance buffered logic analyzer and a programmable signal generator – all in a single probe.

Unique to the System Navigator Pro solution is its ability to concurrently generate input stimulus signals and actively collect real-time trace data. This capability provides the user a self contained in-silicon verification environment allowing concurrent generation of stimulus signal inputs, and monitoring and trace of key signals for an embedded design. The System Navigator Pro series provides a high performance dual mode trace probe with trace bandwidth over 20 Gbps and a high speed trace buffer that can collect up to 2 Gbytes of trace data.

“Analysis for complex SoC designs requires On-chip Instrumentation solutions that can effectively access and store large amounts of trace and related on-chip functional information,” said Rick Leatherman, vice president and general manager, FS2. “We’ve developed System Navigator Pro to enable and facilitate new and more powerful types of on-chip analysis that is key to the successful release of new and more complex silicon products.”

System Navigator Pro Applications

SNP supports tracing processor, bus, or general on-chip systems operations, across either synchronous or asynchronous domains. The SNP architecture is configurable to meet customer needs, with several standard configurations to address multi-processor and multi-bus trace debug. Typical trace collection modes include processor execution, data transactions and embedded bus analysis.

Standard packages supported in the initial release of SNP include PDtrace™, a processor execution and data trace option supported by the MIPS32® 4K®, 24K®, and 34K™ family of cores. The initial SNP release also supports Request-Response Trace (RRT™), a transaction-based OCI architecture for embedded bus analysis. Both PDtrace and RRT can be operated concurrently using dual Mictor connections. The SNP operation is supported by the MIPS third party IP and Ecosystem partners to provide a robust system-level and platform debug tools environment.

The FS2 SNP environment is extensible to heterogeneous multicore debug applications, such as integrated systems analysis of multiple MIPS-Based™ and DSP cores, and trace of OCP, AMBA or custom bus interfaces. Additional applications planned for release in 2007 include additional bus trace support (FS2 Bus Navigator™) and performance analysis support. All applications are or will be supported by FS2's Eclipse-based IDE. Additional customized probe configurations to address specific trace needs or features of a customer design can be rapidly implemented, and such customization of the SNP probe is offered by FS2 as a design service.

Mobileye N.V., a global leader in driver assistance and safety systems for the automotive industry and current 34K customer, has already seen tangible benefits using System Navigator Pro with RRT.

"FS2 solutions based on System Navigator Pro and the Request Response Trace are providing an important and unique capability for Mobileye to analyze system viewpoints and optimize the performance of our EyeQ2 architecture, providing insights that would be difficult to acquire using other analysis approaches," said Elchanan Rushinek, vice president of engineering at Mobileye.

System Navigator Pro Probe (SNP) Features

SNP interfaces to a silicon target via a combination of two 38-pin mictor connectors and a 20-pin JTAG header. The dual mictor interfaces allow a range of trace operations, including split mode, where each mictor can be used to trace asynchronous clock domains. A typical application would be concurrent tracing of asynchronous processor execution and bus operations. The two mictor connections may also be combined into a single high bandwidth parallel trace interface supporting trace widths of up to 72 signals. SNP includes a sophisticated triggering system in the probe, allowing monitoring of combinatorial, sequential or conditional events.

A distinctive feature of SNP is that the mictor connections can be used in a signal injection mode, as well as a signal trace mode, allowing SNP to be used as a digital signal generator to inject patterns, control on-chip operations or write information into a SoC target.

The SNP JTAG interface supports full 1149.1 JTAG operation and JTAG extensions such as MIPS EJTAG at speeds up to a 100 MHz. Both mictor channels and the JTAG interface operate concurrently to allow trace and JTAG control of the silicon target.

The interfaces to SNP are programmable for all JTAG and trace features. SNP includes a high-performance 32-bit processor allowing the 2 gigabyte trace buffer to be searched or preprocessed as a probe level operation, reducing host communication overhead. The probe processor also allows the download of software drivers to improve efficiency of tasks that can be done in the probe at high speed rather than remotely via a communication link to the PC. The SNP to PC Host interface includes high-speed USB 2.0 supporting transfers up to 480 megabits per second. SNP will support a 10/100/1G-Base-T (Gigabit) Ethernet host PC connection.

Pricing and Availability

FS2 System Navigator Pro solution is available now. List pricing of SNP probes starts at \$8995. Contact FS2 or visit <http://www.fs2.com> for information.

About FS2

First Silicon Solutions specializes in hardware verification and debug technologies including on-chip instrumentation, custom silicon IP, development tools and design services for programming, testing and debug of embedded systems in FPGA, SoC, SOPC, ASSP and ASIC designs. FS2 provides full system solutions of IP blocks for processor, logic and complex system-level designs, along with hardware and software tools allowing improved debug and analysis at all stages in the development cycle - from system design and verification to optimized software development. FS2 products enable silicon vendors and their customers to take their designs from "first silicon" to production faster, with a better understanding of the design performance and overall operation - for faster time-to-market and higher quality products. FS2 is a division of MIPS Technologies, Inc.

About MIPS Technologies

MIPS Technologies, Inc. (NASDAQ: MIPS) is a leading provider of industry-standard processor architectures and cores for digital consumer, networking, personal entertainment, communications and business applications. The company drives the broadest architectural alliance that delivers 32 and 64-bit embedded RISC solutions to the embedded market, and in combination with its licensees, offers the widest range of robust, scalable processors in standard, custom, semi-custom and application-specific products worldwide. MIPS Technologies licenses its intellectual property to today's leading semiconductor companies, ASIC developers and system OEMs.

Today, MIPS-Based designs are integrated into millions of products around the world, including broadband devices from Linksys, digital cameras from Canon, DTVs and entertainment systems from Sony, DVD recordable devices from Pioneer, digital set-top boxes from Motorola, network routers from Cisco, and laser printers from Hewlett-Packard. Founded in 1998, MIPS Technologies is based in Mountain View, California, with offices worldwide. For more information, please contact (650) 567-5000 or visit <http://www.mips.com>.

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