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April 7, 2003  
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1. Viewpoint - Exclusive to EDA Alert

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The Productivity Gap

Jackson Kreiter, Chairman and CEO, Hier Design Inc., Santa Clara, Calif.

The EDA industry needs an overhaul! By not properly supporting high-speed, high-complexity field-programmable gate-array (FPGA) designs, traditional EDA vendors are missing out on a huge and growing market opportunity.

Oh yes, EDA software is available to support FPGA design. But it hasn't kept pace with the technological advances in FPGA hardware, and the even more accelerated rate of adoption. These last-generation tools were designed before ultra-deep submicron technologies brought on an explosion in gate count and interconnect delay dominance. Traditional EDA vendors haven't invested in upgrading these tools, thus creating longer runtimes, more design iterations, and a loss in hardware performance.

This has forged a gap in the number of programmable transistors available to FPGA designers and the average number of transistors used by them. The increased number of iterations, sometimes as many as 50

per design, and the time for each iteration (which can last more than eight hours) is nearly undermining the fundamental FPGA advantage -- time-to-market.

FPGAs have long held an advantage over ASICs for both turnaround time and implementation. Now FPGA design starts are surpassing ASIC design starts. Non-recurring expenses (NRE), prolonged time-to-manufacturing, risk of respins, and high inventory costs push ASIC designers and their managers to re-assess FPGAs. Compelling FPGA technology breakthroughs, such as 10-million-gate densities, 400-MHz clock speeds, and 300-mm wafers, have made it almost impossible for design houses to justify an ASIC over an FPGA implementation.

Finally, ASIC production volumes and the price per part, which was once more cost-effective than an FPGA implementation, have risen consistently over the past few years with each technology shrink. Conversely, FPGA pricing drops with each new technology, making an FPGA implementation more viable and sensible. The ASIC to FPGA migration is underway.

Armed with this information, the EDA industry must act quickly to support its customer--the electronics design engineer. High-speed, high-complexity FPGA designs hold the promise for the next big market opportunity for EDA.

Contact Jackson Kreiter directly at: <mailto:jackson@hierdesign.com>

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2. News

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EDA Industry's 2002 Revenues: \$3.7 Billion

EDA industry revenues for Q4 2002 were \$907 million, 13% less than Q4 2001, according to the EDA Consortium's (EDAC) Market Statistics Service (MSS). Total EDA industry revenue in 2002 for products, maintenance, and services was \$3.7 billion, a 7% decrease from 2001. Product and maintenance revenue -- including CAE, IC physical design & verification, pc-board and MCM layout tools, and semiconductor intellectual property -- totaled \$3.4 billion, 3% less than 2001.

"EDA revenue for 2002 suffered a modest decline," says Walden C. Rhines, EDA Consortium chairman, and chairman and CEO of Mentor Graphics Corp. "However, given the global downturn in the semiconductor industry, a relatively small decline indicates that EDA remains essential to getting new products to market, and is generally less susceptible to overall industry volatility."

Last year was the first time reported revenue hadn't increased year-over-year since the EDA Consortium began its Market Statistics Service in 1994.

In Q4 2002, reporting EDA companies employed 18,100, 6% less than at the end of 2001.

EDA Consortium ==> <http://lists.planetee.com/cgi-bin3/flo/y/eQMw0FrrzE0BSK0puL0A1>

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### 3. News

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#### OCP-IP Gains Alcatel, Amphion As Members

The Open Core Protocol International Partnership (OCP-IP) added two new members to its roster: Alcatel and Amphion Semiconductor Inc. Membership in OCP-IP allows both companies' customers to optimize design resources and shorten design cycles, which ultimately will lower design costs and bring products to market faster.

"Open, common IP interfaces will become increasingly important as the industry continues to move toward complex SoC designs, and that is the way to reduce risk and time to market for our new SoC designs," says Thierry Pfirsch, core competence manager of Alcatel Hardware Coordination. "As OCP-IP's mission is to develop a standardized socket for plugging IP cores into SoC designs, it offers the first truly open effort to make plug-and-play SoC design a reality."

"There is clear value to an industry-standard socket that eases the process of complex SoC design by promoting IP core reusability and reducing design time, while at the same time lowering both cost and risk," says Stephen Farson, Amphion's vice president of engineering. "OCP-IP offers the first truly open effort to make plug-and-play SoC design a reality. We are pleased to support its efforts."

OCP-IP ==> <http://lists.planetee.com/cgi-bin3/flo/y/eQMw0FrrzE0BSK06fk0AK>

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### 4. News

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#### IBM Relies On Tera Systems To Extend ASIC Technology

The TeraForm RTL Silicon Virtual Prototype (SVP) has been integrated into the IBM Blue Logic MidRange ASIC design flow, which supports a new engagement model allowing register-transfer-level (RTL) handoff of customer designs. IBM and Tera Systems Inc., creator of the SVP, jointly developed and qualified the flow.

"In the past, IBM has focused on the high end of the ASICs market. With this new methodology, we are expanding our focus beyond high-end applications," says Tom Reeves, vice president of ASICs, IBM Microelectronics Division. "Through our joint work with Tera, we are now delivering this new methodology to customers who want the security of working with IBM on mid-range designs with an RTL handoff-based flow."

TeraForm is used on customer designs upstream from synthesis to identify potential timing, area, congestion, and design-closure issues early in the design cycle at the RTL. This leads to better predictability and shorter time-to-market. The TeraForm-IBM flow delivers predictive analysis, enabling early visibility into issues like critical-path timing violations and routing congestion while the RTL is being written. This, in turn, will alleviate time-consuming late-stage design iterations.

Tera Systems ==> <http://lists.planetee.com/cgi-bin3/flo/y/eQMw0FrrzE0BSK06K70Az>

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5. Happenings

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9th IEEE/DATC Electronic Design Processes (EDP) Workshop Monterey Beach Hotel, Monterey, Calif. April 21-23, 2003

<http://lists.planetee.com/cgi-bin3/flo/y/eQMw0FrrzE0BSK08eh0AI>

24th Zuken Users Group North America  
Phoenix, Ariz.

April 27-29, 2003 <http://lists.planetee.com/cgi-bin3/flo/y/eQMw0FrrzE0BSK08en0AO>

1st Zuken Users Group Europe  
Veldhoven, The Netherlands

May 19-20, 2003 <http://lists.planetee.com/cgi-bin3/flo/y/eQMw0FrrzE0BSK08ej0AK>

40th Design Automation Conference  
Anaheim Convention Center, Anaheim, Calif.

June 2-6, 2003 <http://lists.planetee.com/cgi-bin3/flo/y/eQMw0FrrzE0BSK08ek0AL>

DesignCon East 2003

Royal Plaza Hotel and Trade Center, Marlborough, Mass.

June 23-25, 2003 <http://lists.planetee.com/cgi-bin3/flo/y/eQMw0FrrzE0BSK08el0AM>

EuroDesignCon 2003

Arabella Sheraton Grand Hotel, Munich, Germany

October 27-30, 2003 <http://lists.planetee.com/cgi-bin3/flo/y/eQMw0FrrzE0BSK08em0AN>

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