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#### About This Issue



## Musings at MIT

*A sanctuary for restless intellect and disorganization*

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September 1-5, 2003 **By Peggy Aycinena**

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The best thing about MIT is the Charles River.

The mile-long campus of the **Massachusetts Institute of Technology** is both defined and constrained by the gently flowing waters of this ancient river, which grows broad as it passes under the bridge at Mass Ave - the portal to Cambridge and MIT.

Within its dark stately flow, the leafy conceits of Harvard and the urban sensibilities of Boston University mingle with the ascetic intellects of MIT and the tasteful energies of Boston's Back Bay. The river moves on downstream and adds the gritty working class accents and vaguely puritanical

and democratic ideals of downtown Boston to the flow before joining with the Mystic and passing grandly through Boston Harbor and on out to the chilly waters of the Atlantic and rugged realities beyond.

MIT is a place within context, anchored to the soil of Cambridge by the silent, heavy symmetry of the dome and its pillared, orderly attendants that evoke the names of Archimedes, Newton, Franklin, Brahe, Gutenberg, Plato, Des Cartes, Fulton and others. The dome wants you to believe that this place is a shrine to mathematicians, scientists, and engineers stretching back through history - male, confident, and proud.

But don't be fooled by the public face of MIT. Behind that classical façade, it's a place of chaos and industriousness, disorder and irregular, non-linear progression toward real solutions to real problems. It's a place where the elegant proof meets the unruly world and designs are optimized within an acceptable tolerance level.

It's a campus that was founded on applied technology, where the basic sciences arrived late, and where a hostile take-over bid by erudite Harvard in the early 20th century failed because MIT was unwilling to play second-fiddle to cerebral theory and the ivory tower. It's a place where people with a passion for the sciences are mandated to get their hands dirty. It's a place where boys can be boys - and now, happily, girls can be girls - if that means thinking and scrambling and making a mess in order to understand what's what in the world around us. It's a place where there are six major areas of study numbered I to VII.

On a rainy September morning, I found the Computer Science Department at MIT and Professor Srinivas Devadas by wandering past the disarray of the emerging Stata Center on campus, soon to be home to both the EE and CS Departments. The disarray of Stata is not due to the army of construction equipment and people vainly attempting to meet their year-end completion deadline for the building. The disarray is designed right into the structure, which is suffering - or celebrating - from a distinct lack of vertical lines or right angles. Very MIT.

When I reached Dr. Devadas a block later in Technology 100, he was hunkered down over his computer trying to sort out a Windows problem, which was a nice way to meet one of the best and brightest of MIT and EDA.

Good to know that accolades and accomplishments notwithstanding - PhD in CS at the tender age of 24 from U.C. Berkeley, NSF Young Investigator Award (1992), Best Paper Awards from both IEEE

Transactions of VLSI Systems (1996) and Computer-Aided Design (1990), Best Paper Award at DAC (1998), Fellow of the IEEE (1998), author of *Logic Synthesis* with Ghosh and Keutzer, and now Chair for MIT's Area II - Srinivas Devadas suffers from the same, mundane irritations that the rest of us enjoy when dealing with the sloppy code that emanates from Bellevue, WA.

Dr. Devadas has been on the Computer Science faculty at MIT since he finished at Berkeley in 1988. During his time at Berkeley and in the years following, he was extremely busy, along with his peers, sorting out many of the challenges in computer-aided design of logic systems and their ilk.

Since the late 90's, however, Devadas, has wandered away from his early passion for EDA and today teaches undergraduate classes and sponsors graduate research that more closely mirror his current interests. He's busy teaching what he's preaching - that a strong foundation in math, computer science, and electronics are all necessary to understand the modern world.

He told me: "In the early days it was really exciting in EDA. Cadence was just starting, and Synopsys as well. When I started, people were working on logic design, layout, schematics, RTL, behavioral synthesis. It was beautiful from an academic point of view. There were a good 10 years in there, but those days are past."

"Since that time, EDA has grown into a \$3 or \$4 billion dollar industry that's [fully] mature. Now it's not about levels of abstraction, but about getting that last 10% of functionality out of the existing tools. That's fine for R&D in industry, but not in academia. Today it's hard to do cutting-edge research in EDA, hard in academia to improve upon the R&D being done by corporations and companies. There are some new areas in EDA, a couple of nice ideas, but the experimental set-up is so expensive that EDA's kind of losing it at this point. It's too hard and too boring. People tend to work on things that they're comfortable with, so dramatic change in a mature industry is rare. It's about the aesthetics of the problem for me, and it's just not there [anymore in EDA]."

"In academics, you define a problem and work on challenges that are not necessarily important to industry. Once a problem is established, industry will take over. In academia, however, it's nice to enjoy the problem for a while [before that happens]."

"So I decided I didn't want to work on [existing] CAD problems anymore, but wanted to work on a high-performance processor, which has its own painful set of problems. But for a number of reasons, I decided instead to work on building a processor that isn't high performance or low power, but is a secure processor - one that would protect against network attacks and copyright issues. This is

[allowing me to address] problems that are broader than just EDA. It's nice to do EDA for that particular type of system, but there are generic EDA tools available - the companies have done a good job of providing useful tools to support the work."

"I took a year's leave, 2000 to 2001, to work at Sandburst Corp. [Devadas served as Principal Engineer at the fables start-up founded by MIT's Arvind, Johnson Professor of Computer Science and Engineering.] However, for many reasons, I just didn't enjoy it. We've got VCs walking around the halls all the time here at MIT, but after my [recent] experience in industry, now I just get up and shut my door when I see them running by. I made the decision when I came back to MIT in 2001 that I would be a scholar for another 10 years before I ever considered leaving again."

"[Meanwhile], after Jonathan Allen died [Professor and Director of MIT's Research Lab of Electronics], our VLSI design course kind of went dormant - from 1999 until 2002 or so. It's true that VLSI design can be seen to be somewhat of a trade skill, perhaps inappropriate [to some] for the atmosphere at MIT. However, we know that the subject is important and we're in the process of reviving the course. We're making the course more modern, to teach about FGPA's and new synthesis tools. These are important things for people to know."

"Meanwhile, I've decided to concentrate on teaching undergraduates - in particular, freshman and sophomores. We've got very sharp undergraduates here at MIT and I really like the younger students. They're not [jaded] like the older students."

"I'm teaching a basic course on Java, and one on Boolean logic, and one on hardware. I've become interested in the power of the material and am interested in how to teach students to think [simultaneously] across all three disciplines - mathematics, software, and hardware. If students don't think about math, software, and hardware at the same time, they're starting off [on the wrong foot]. Right now the CS department and EE departments are in different buildings on campus. When we're all [housed together] in the new Stata Center, it will help us to think about embedded systems, across hardware/software [boundaries], reusable IP, behavioral synthesis, SystemC."

"Right now, I'm seeing a lot of crummy CAD coming out of the systems area and the conferences aren't helping. The CAD guys go to their own conferences and have good CAD, but crummy designs. The Design guys are off at their own conferences and have good designs, but crummy CAD. People see the same faces at their own conferences, a small group of guys that they're comfortable with. They [resist] going to conferences where they don't know anybody and they're not known. I want to go to conferences where people don't know me and I'm trying to do that more these days."

"DAC could improve if it would move beyond CAD. I know the designers are there, but it's only the ASIC guys who come - people who want to write Verilog and are looking for tools to attack the Verilog and the gates. But DAC needs to [encourage] the systems architects to come as well. It should be combined with ISCA [International Symposium on Computer Architecture], which is just as old as DAC and about the same size [short of the commercial exhibits]."

"I don't like theorists. They don't know how to build things. Here at MIT we want our students to know how to handle problems, to get their hands dirty. We want them to think in an organized way. The best training for organized thinking comes with mathematics - a good computer science student should know how to do a proof. The best student I've ever had recently finished his Masters Thesis here. He came out of the Ecole Polytechnique [France] and knew how to prove a theorem, how to code, how to hack an operating system, how to design an FPGA. His background was excellent. American students could be [educated similarly], but it takes too much discipline in the high schools and colleges to force students to [tackle all the disciplines]."

"My job here at MIT is the best job in the world. I get really wired just by hanging out with young people and I tell them all the time, 'Don't be like me! Don't get conservative! You need to show leadership, pursue innovation, take risks! Get your hands dirty!'"

Very MIT.

**(Editor's Note:** By the way, don't get me wrong. MIT is no Stanford. It snows at MIT. Of course, nobody ever disassembled a police cruiser and re-assembled it on top of Hoover Tower. Maybe it *should* snow at Stanford!)

### ***Industry news - Tools and IP***

**Cadence Design Systems, Inc.** and **IPCore Technologies Co., Ltd** (Shanghai, China) announced that they have cooperated to develop the first digital design kit for CSMC's process. CSMC is the **Central Semiconductor Manufacturing Corp.**, which offers IC manufacturing foundry management and operating services for China and the international markets. The companies say that the kit has been developed based on CSMC's CMOS process technology and validated with real customer designs. Cadence says it is the first EDA company to integrate the silicon design chain for

CSMC and IPCore through this RTL-to-GDSII digital design kit. Per the Press Release, Yi-Chen Zhao, Vice President for Engineering Services at IPCore, said, "IPCore is a leader in the ASIC design services market in China and has an advanced design methodology to meet design challenges down to 0.18 microns. There is a large market for a mature technology worldwide, especially in China. So we chose Cadence advanced nanometer design tools as our design service platform and collaborated with Cadence to develop the digital design kit for the CSMC process in order to meet the needs of these customers for design efficiency and quality."

**Esterel Technologies** announced Esterel Studio 5.0, which the company says is a "comprehensive tool suite for the design and verification of complex consumer and multimedia SoCs. Esterel Studio 5.0 lets the user capture a design specification and then automatically generate the hardware description in HDL-RTL or C. Combining advanced simulation methods with a sophisticated proof engine, high level primitives and hierarchical state machines, Esterel Studio 5.0 builds verification into the design process, eliminating the majority of functional errors right at the start of the design process and allowing engineers to develop a golden reference model in text and/or graphics with a complete path to correct-by-construction, automated implementation. Early adopters have already used the technology for production designs and FPGA prototypes."

**Mentor Graphics Corp.** announced that **Texas Instruments** has adopted its Hi-Speed USB On-The-Go (OTG) IP. Per the Press Release, Dave Pahl, General Manager for Digital Camera Products at Texas Instruments, said: "We selected Mentor Graphics as our OTG provider since they have a history of delivering high quality IP solutions and are committed to industry standards and certification. As a result, this reduces our risk in delivering quality products to our customers, knowing that the IP cores have been pre-tested and directly validated against the standard." (See *Newsmakers* item below.)

Also from **Mentor Graphics** - Accelerated Technology, the Embedded Systems Division of Mentor Graphics, announced a version of the Nucleus RTOS for the VC01 processor from **Alphamosaic Ltd.** The companies say that "embedded developers in the mobile market now have a video processing platform that they can use to bring video to wireless applications including digital still and video cameras, mobile videophones, and camera-enabled PDAs. The VC01 is a low power, fully programmable processor based on VideoCore technology. The VideoCore architecture supports extremely fast functions for multimedia and video processing allowing higher quality video to be available in wireless devices without impacting battery life."

**Novas Software, Inc.** announced that **Global Unichip Corp.** has adopted Novas' Verdi Behavior-

Based Debug System as the standard debug and design exploration platform for their ASIC products. The companies say that Verdi has also been "deployed" across multiple IP design teams in Unichip.

**Synopsys, Inc.** announced the release of a synthesizable, configurable 6811 8-bit microcontroller into the company's DesignWare Library. The company says the 6811 MacroCell is intended for designers who need a "drop-in, industry-standard embedded 8-bit microcontroller with broad software tool chain support. This solution should also appeal to those designers who are migrating from a discrete 6811 chip to a SoC implementation."

CoWare Inc. announced that the first processor support package (PSP) using the ARM11 Cycle Callable Models (CCMs), has been added to its ConvergenSC Model Library. Coware says the PSP for the ARM1136J-S core will help reduce overall design time by allowing designers to explore and debug their designs at the system level. The ConvergenSC Model Library of simulation models for SystemC includes models based on ARM certified CCMs. In addition to the ARM1136J-S core, the library includes the ARM7 core, the ARM9 core, and the ARM10 core families, as well as numerous other processor and bus models.

**Summit Design, Inc.** and **ARM** announced that Summit has extended its EDA Partnership agreement with ARM and has licensed the ARM Cycle-Callable Models (CCMs) for distribution with Summit's Visual Elite ESC product. Summit describes Visual Elite ESC as a SystemC-based hardware/software, co-design and co-verification environment with integrated Instruction Set Simulator (ISS) models for target processors. ARM CCMs are transaction-accurate simulation models of ARM processors, designed to be easily integrated with custom cycle-based simulators. Each CCM contains a high-speed cycle-based behavioral model, an ARM debug interface and ARM memory interface. The companies say that Visual ESC's high-level design methodology, together with its tight link into the ARM CCMs, will offer developers a design strategy for faster development of complex next-generation products.

I had a chance to speak with Rami Rachamim, Director of Marketing at Summit, from his office in Israel on September 3rd: "This announcement is an extension of the ARM agreement we've had regarding co-verification, but now we're including the new CCMs and integrating those models into our Visual Elite system. This will allow users - customers and engineers - to run complete hardware/software environments and leverage performance and a unified language [SystemC] in a hardware/software domain."

"The idea of hardware/software co-design is definitely at an early stage, which is a reason for the

entire industry to adopt this migration. The [strategy] needs a lot of modeling on the hardware side, and requires a psychological effort to bring the software and hardware guys together. Even today, within the same company, many times software and hardware people are not interacting. SystemC is making for a change here, however."

"Until SystemC, if you were to go into large companies, you would see them using C/C++ based simulations and running simulations with software in early stages [of a project]. But when SystemC came along, it brought a standard for the hardware guys, which - though still not mainstream - is definitely bringing an improvement [in the way things are done]. We've seen things develop quickly over the last four years - particularly at DAC - and I do think there is a change underway. Now we're actually seeing companies like Motorola and National [Semiconductor] doing tape-outs with SystemC."

"It's true that moving into new methodologies [like SystemC] requires an investment risk, and people are being very cautious today [in the current economic environment]. But people are finding that they need new ways to do things - particularly on the physical side where nanometer technologies [are demanding change] - and engineers today are providing us with a positive change in the industry."

"I think the biggest challenge for customers in the industry currently is the modeling issue. In order to leverage whatever SystemC provides, we really need to provide complete platforms. And in order to provide platforms, we need the modeling to support it. It's going to be the biggest challenge to the industry and not something that just one company can provide. The solution is going to have to come from different levels and different companies and it's going to require an investment."

"Similarly, on the architectural side of things - the side that's getting a lot of attention these days - engineers need to be able to estimate the performance metrics for their environment. Multiple systems environments will need architectural exploration and modeling - both are important issues and not something that every engineer is using. But they will definitely be something that will become more useful [as we move forward]."

### ***Coming soon to a theater near you***

**Denali MemCon** - The company describes this two-day conference as "the industry's premier event

for leading-edge trends in the business and technology of semiconductor memory." If they're right, you should go. It's in San Jose at the Westin Hotel on October 7th and 8th, and includes over 25 presentations from industry experts, including representatives from the various sponsoring vendors. Tom Reeves from IBM Microelectronics' ASIC Product Group and Bill Jennings from Cisco Systems' Routing Technology Group will be giving keynotes. Note that if you're going to be in Tokyo on September 11th and 12th, the conference will be happening there before the San Jose event in October. ([www.memcon.com](http://www.memcon.com))

**Chartered Technology Forum** - Save September 18th and try to get to the Double Tree Inn in San Jose, CA, for this all-day event. Yes, it's true that **Chartered Semiconductor Mfg.** is sponsoring the event, but there's generic learning to be had there as well. Among this year's speakers, you'll find Bernard Meyerson, **IBM** Fellow and Chief Technologist at the IBM Technology Group. His topic will be: "Driving Innovation: A Business Imperative for Silicon Technology."

Lest you think Meyerson's talk threatens to restate the obvious, the Forum Organizers say, "In the past several years, with the increasing challenge to scaling, innovation has played an increasingly important role in the progress of modern semiconductor technology. The introduction of Copper interconnects, Silicon Germanium devices, Silicon on Insulator technology, and numerous smaller materials-based enhancements, have all facilitated progress in semiconductors. Going forward into the future, such innovation moves from the role of simple technology differentiator to that of being a business imperative, required for survival. Dr. Meyerson will explore the origins of the need for this transition, and discuss several unusual strategies for device technologies demonstrating extraordinary dimensional and energetic characteristics." Good stuff. ([www.charteredsemi.com](http://www.charteredsemi.com))

### **Newsmakers**

**Editor's Note** - In case you missed it, go read [Russ Henke's](#) detailed analysis, "What did the Last Quarter bring?" It's posted on EDAToolsCafe and is a great read for all involved in the industry.

**Applied Wave Research, Inc.** (AWR) announced the appointment of additional sales representation in Europe and Asia. Under the terms of the agreements, **Kataros Co. Ltd.**, and **Euan Information Technology** in Korea, **eVision Systems GmbH** in Germany, and **Setup Electronica** in Spain will provide electronic systems and IC designers with AWR products and support.

**Camstar** announced that **Finisar Corp.** has chosen Camstar's InSite as the standard throughout its worldwide manufacturing sites in the United States, Malaysia and Singapore.

**Carbon Design Systems** is opening its doors in Waltham, MA, and announcing the delivery of software products that enable system validation of hardware and software in an enterprise-wide environment. The Press Release says, "For the first time, critical software drivers, firmware, and diagnostics runs at KHz execution speed on the 'golden' RTL hardware model with cycle and register accuracy. This enables system and customer validation to occur much earlier than traditional methods." Carbon says its first products target the pre-silicon system validation market.

Meanwhile, the company also announced over \$5 million in funding from **Flagship Ventures** and **Commonwealth Capital** to commercialize its technology. Carbon's executive team includes Stephen Butler, President and CEO; Kevin Hotaling, Vice President of Worldwide Sales; and Bill Neifert, CTO. The company was founded in April 2002. Steve Ricci, Managing Director and Vice Chairman of Flagship Ventures, is quoted: "We are excited about the progress Carbon has made over the last year in assembling a stellar team and capturing early revenue. With the explosion in chip software content and gate counts, Carbon is uniquely positioned to address an industry wide problem in a largely untapped market."

**Circuit Semantics, Inc.** (CSI) announced that it has closed a \$1.6 million funding round. The company says that current investors **VenGlobal** and **Crescent Ventures** led the round. In addition, the company announced that it has moved its headquarters to Mountain View, CA.

**IBM** announced: "The **Accellera** EDA standards organization has approved Property Specification Language (PSL) 1.01 as an official standard. PSL, based on IBM's Sugar language will advance assertion-based verification in simulation and formal verification, the two prevailing techniques for assuring the correctness of chip design prior to fabrication. More than 40 individuals representing over 20 companies participated in the efforts to form the PSL standard from its Sugar basis. PSL is a language for the formal specification of hardware and is used by engineers to specify the functional properties of logic designs. These properties, in turn, serve as input to property-checking tools, which are key to modern-day functional verification. More and more EDA companies are supporting verification tools driven by PSL. To support the growing adoption of the language, IBM provides an open source Sugar parser to tool developers."

Accellera Chairman Dennis Brophy is quoted in the Press Release: "The approval of Accellera's PSL standard, based on IBM's technology contribution, is a significant milestone for Accellera and

improves the productivity of designers doing system-level design and verification. Accellera members and the PSL technical team have done an outstanding job to get PSL ready for deployment."

**Integre Technologies** and **Tower Semiconductor Ltd.** announced that Integre has joined Tower's Authorized Design Center program. Integre is the first affiliate in North America. Tower says Authorized Design Centers are established to link Tower with IC design firms to provide customers with support for the Tower semiconductor fabrication flow.

**USB Implementers Forum (USB-IF) Compliance Workshop** - The workshops are held regularly to promote USB product development, validate product compliance with the specification, help foster communication between product manufacturers, and ensure that USB Peripherals operate together. Organizers say the three-day event evaluates products against the standard for Full Speed OTG with exacting tests for device interoperability, as well as ensuring strict electrical and protocol compliance. The following news items from Mentor Graphics and Synopsys hail from this event.

**Mentor Graphics Corp.** announced that two of its USB On-The-Go (OTG) IP cores achieved compliance certification at the **USB-IF Compliance Workshop** held in Milpitas, CA, in early August. The company said this was the first opportunity to test the Mentor Graphics Full Speed (MUSBFDR) and Hi-Speed (MUSBHDC) Dual Role Controllers against the OTG standard, and that "the certification validates the quality of Mentor Graphics IP and allows developers to integrate the company's cores with the utmost confidence, enabling the rapid creation of OTG applications."

Similarly, **Synopsys, Inc.** announced that it has received the "industry's first" **USB-IF** certification for its DesignWare Cores USB 2.0 PHY (physical layer) IP. The company says the certified core supports all USB 2.0 speeds - high speed, full speed, and low speed - and is compliant with the USB 2.0 Transceiver Macrocell Interface (UTMI+) specification. The company also says, "The certification means that SoC designers can implement fast USB interfaces in deep-submicron geometries."

Also from **Mentor Graphics** -The company announced that **Intrinsix Corp.** has joined its FPGA Advantage Solutions Thrust (FAST) Partner Program. The FAST Partner Program provides partners with access to Mentor Graphics FPGA Advantage tool suite, and FPGA design methodologies, training, and certification from Mentor Consulting.

**Monterey Design Systems** announced that **Nokia Venture Partners and Information Technology Ventures** have made investments in the company. These new investments bring the total series II funding round to \$15 million. Previously announced investors in this round include

**Sevin Rosen Funds, Excelsior Venture Partners III LLC, RHO Management Trust, Lucent Venture Partners, Kaufman LLC, and Vertex Partners.** W. Peter Buhl, Partner at Nokia Venture Partners, is quoted in the Press Release: "Monterey is quickly emerging as the technology pace setter in design planning and prototyping. Effective planning and prototyping leads to smaller, faster, less power-hungry chips, more predictable design schedules, and lower engineering costs."

**Open Core Protocol International Partnership (OCP-IP)** announced that **STMicroelectronics** has joined the organization. ST is a Governing Steering Committee (GSC) member, and is a participant in OCP-IP's Working Groups. As a member of the GSC, ST will be part of a team of GSC members including **Nokia, TI, Sonics, and UMC**, among others. OCP-IP says that Working Groups are charged with the task of developing enhancements and support for OCP, and addressing the future needs of the membership in the use of the specification. The group recently announced the availability of the OCP 2.0 Specification Release Candidate. OCP-IP provides a common standard for IP core interfaces (sockets) that facilitate plug-and-play SoC designs. OCP-IP members receive free training and support, free software tools, and free documentation, which the organization says allows members "to focus on the challenges of SoC design."

In related news, **Imagination Technologies** and **OCP-IP** announced that Imagination Technologies has joined the OCP-IP. John Metcalfe, Vice President for PowerVR Business Development at Imagination Technologies is quoted in the Press Release: "OCP-IP's industry standard socket enhances IP core reusability and reduces design time for complex SoCs while also lowering both cost and risk. This can be of major impact in the competitive SoC IP market where design time and cost effective utilization of IP are highly important."

**OCP-IP** also announced that **eInfochips** has joined the organization. Additionally, eInfochips announced plans to make their IP cores OCP2.0 compliant, and says the company is in the process of developing an OCP2.0 eVC using Specman Elite, to support verification of IP Blocks and SoC designs for compliance with OCP.

**Sequence Design** presented its first annual *Powerhouse Design Award* to Tensilica at a ceremony recognizing the company's contributions to low-power IC design. The award was presented to Tensilica's Himanshu Sanghavi, Hardware Engineering Manager, who said low-power dissipation is an important design goal of his company. Sequence says that, going forward, it will annually honor the design team whose efficient approach to power management serves as a model for every engineer struggling with the same issues.

**O-In Design Automation** announced that it has been granted U.S. Patent Number 6,609,229, entitled "Method for automatically generating checkers for finding functional defects in a description of a circuit," which covers methods of specifying and generating assertions for use in simulation. Products currently being shipped by O-In incorporate the methods and technologies covered by the newly granted patent. Per the Press Release, Curtis Widdoes, Chairman and CTO at O-In, said, "Very early on, our customers told us that it was critical to make assertions easy to use. With their guidance, we developed a wide range of methods and technologies for design engineers and verification engineers to easily specify and use assertions. The newly granted patent covers those methods and technologies."

### *In the category of...*

#### **The cruelest month**

Millions of housewives are regularly portrayed in detergent commercials as blissfully relieved when September arrives and the kids are finally back in school. The house is peaceful and the woman free to attend to her cleaning, her coffee klatches, and her beloved soap operas. Of course, as with every other insipid fantasy perpetuated by the domestic-products marketing machine, there's nary a shred of truth in any of the Happy Housewife drivel.

More likely, the woman in question has been juggling camps, babysitters, and 3-day weekends stolen from a way-too-busy workweek all summer long in order to deal with child care and child rearing issues. And, rather than being relieved at summer's end, she (and her male counterpart) are left with a vague sense of unease that another summer has come and gone with too little family time and too few relaxed hours with children who insist on growing up and away - way, way too fast and furiously.

And so it is in our household as the summer draws to a close. But for us, this September is a particularly poignant one. Our youngest has just left for college for the first time, all three of them now being in college or graduate school, and as much as I dislike the term, suddenly our house is an 'empty nest.'

We're slowly becoming accustomed to this new state of affairs, although the silence and orderliness around us is deafening. The phone is no longer ringing off the hook, there are no piles of laundry

lying about, no more empty dishes, bowls, cups, etc. sitting on bedside tables, no more newspapers and magazines strewn about the kitchen table, no more running shoes and sweatshirts and baseball gloves on the floor next to the front door, no more rowdy arguments about politics, ethics, music, or religion at the dinner table, no more high school and college friends coming and going at all hours of the day and night. In other words, our household - now that this past merry, unorganized, and lively summer is over - no longer feels like a frat house.

Perpetual quiet has set in and, rather than being relieved, we're left staring at the door and struggling with a vague sense of unease that all of the child-rearing years have come and gone with too little family time and too few relaxed hours with children who have insisted on growing up and away - way, way too fast and furiously.

Of course, this is a rite of passage that every parent goes through, and we'll survive it as so many have before us. We'll move on to the next phase of life. We'll enjoy the extra time and peace and quiet. We'll try not to look back and wish for the 'good old days' when they were all young and innocent and safe under our roof. We'll hope they remember to call home and let us know how they're doing. We'll listen for news of their triumphs and tragedies. In other words, we'll show the same level of dignity and independence that our own parents exhibited when we waved goodbye and never looked back so many years ago.

September is indeed the cruelest month.

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