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Stone axes, soldering guns, and SoCs

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George Santayana observed, "those who cannot remember the past are condemned to repeat it." And system on chip (SoC) designers who fail learn that truth do so at the peril of their careers.

We are in a similar situation that occurred in the late 1950's, before integrated circuits. Small computing systems usually required thousands, if not tens-of-thousands, of individual hand-soldered connections because they used discrete components — transistors, capacitors, resistors, and diodes. T. R. Reid's classic history of the integrated circuit, *The Chip*, documents how Bob Noyce, co-inventor of the integrated circuit viewed the problem:

"Here we were in a factory that was making all these transistors in a perfect array on a single wafer and then we cut them apart into tiny pieces and had to hire thousands of women with tweezers to pick them up and try to wire them together. It just seemed so stupid. It's expensive, it's unreliable, it clearly limits the complexity of the circuits you can build. It was an acute problem. The answer was, of course, don't cut them apart in the first place. But nobody realized that then."

The inherent unreliability of those hand-soldered connections posed an increasingly intractable and insurmountable problem that became known as known as the interconnection problem, or Tyranny of Numbers. But it is only slightly different today since the semiconductor industry increasingly faces a new interconnections problem variant. Now, instead of the challenge of integrating large numbers of discrete components, designers grapple with integrating already large, and increasing, numbers of IP logic blocks into System on Chip (SOC) designs.

Here we are designing increasingly complex SOCs with shorter time-to-market deadlines. Yes, we are using large numbers of IP cores. But, each IP core has a different interface. So, for each SOC design, we have to haggle about how to integrate all those interfaces.

It just seems so stupid. It's expensive, it's unreliable, it clearly limits the complexity of the circuits you can build. The numbers of different interfaces in some of these circuits are just too big. It is an acute problem. The simple fact is that you cannot do everything that an engineer wants to do within these shrinking schedules. The answer is, of course, use one configurable standard IP core interface.

Yesterday's interconnections problem solution was the integrated circuit. Today's interconnections problem solution is a standard IP Core interface known as the Open Core Protocol — OCP.

OCP is supported by the OCP International Partnership (OCP-IP), which has dozens of members, an impressive steering committee, and highly active working groups run by industry leaders. Make no mistake about it, OCP is the reigning lingua SOC for rapid time-to-market designs. OCP is very straightforward, allowing you to master its concepts in a few well-invested hours. You can request the new OCP 2.0 specification for research purposes at no cost from the [OCP-IP web site](#).

Since OCP has achieved critical mass, OCP 2.0 fluency has become an increasingly valuable industry skill. Of course, OCP 2.0 design skill will be better. Mistakes of the past are best left behind.

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