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[EDA Alert]

EDA Alert: November 30, 2004

David Maliniak
ED Online ID #9281
November 30, 2004



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EDA Alert e-Newsletter
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- Not very
- Moderately
- Significantly
- A real problem
- Hope we can

Electronic Design's Quick Poll ==> <http://lists.planetee.com/cgi-bin3/DM/y/e>

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1. Viewpoint -- Exclusive to EDA Alert

Combating The Complexity of IP Tagging

Ian R. Mackintosh

Chair, IP Protection Pillar and Board Member, VSI Alliance,
Wakefield, Mass.

President, Open Core Protocol International Partnership,
Mountain View, Calif.

The frenzied activity surrounding SoC development, particularly in the digital consumer arena, has reduced many product-version lifecycles to 12 months and, often, seasonally less. With first-time design-success reports ranging from 40% to 70%, it's more critical than ever for product design cycles to be made more robust and debug cycles dramatically shorter.

Leading companies have highlighted the need for a standardized approach to track IP blocks (or virtual components) used in SoC design and manufacture. The challenge is to revolutionize all record keeping about IP blocks, from the blocks' inception, through the high-level RTL design process, and down into the final GDSII database.

A standardized solution has been devised and is now promoted by VSIA. The standard, entitled "Soft IP Tagging Standard Version 1.0" (IPP 4 1.0), unifies the complex landscape of custom design flows, proprietary tools, and myriad suppliers to align the entire user community tied to IP. The scheme benefits IP developers and resellers as well as SoC designers, and efficiently provides essential data to the product engineering and manufacturing engineers responsible for ramping up complex SoCs to production.

The tagging method allows identification information to be taken from the IP source file and provides a process for passing this data through each chip-level design step, including synthesis, timing, placement, routing, and others. This ultimately leads to generation of the chip's GDSII representation. At each level, tracking information is obtained from the previous level and transported to the next level using the prescribed output format. Such an approach keeps the infrastructure independent of the design methodology, design tools, and EDA providers.

Information includes identification, vendor ID, and most importantly, version specifics. Thus, designers can explicitly identify the version of a piece of IP (or VC), even after it has been absorbed into an overall "sea of gates" for the chip. As a result, everyone in the design infrastructure receives direct benefits. Foundries can provide additional services and quality checks before manufacturing, while VC providers document version and date information crucial for quality and business purposes. EDA suppliers are able to enhance their tools to support an industry-standard format and provide software to collect, correlate, and display information at convenient places in the tool chain.

The visibility of such information during the design phase will itself reduce the chance for errors. As for that nightmarish debug phase, the right data can now be readily available in a convenient, standard format. The new Soft IP Tagging scheme from VSIA will be a great assistance in getting designs into production and meeting those critical, steep manufacturing ramps.

Contact Ian Mackintosh at: <mailto:ian@ocpip.org>

To comment on this Viewpoint, go to Reader Comments at the foot of the Web page:

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<http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw0BSK0BNFo0As>

2. News

Kit Readies Design Flow For 90-nm Process

A fully validated RTL-to-GDSII design enablement kit for the 90-nm process jointly developed by IBM and Chartered Semiconductor Manufacturing is now available online. The kit, from Magma Design Automation, includes technology files, a methodology guide and scripts, and Magma-qualified libraries. When used with Magma's Blast Create, Blast Plan Pro, and Blast Fusion products, the kit allows designers to immediately begin developing SoCs for dual-source manufacturing at IBM's and Chartered's 300-millimeter facilities.

A reference methodology kit, which contains a methodology guide as well as scripts that enable users to run the entire RTL-to-GDSII flow smoothly and predictably, is available from Magma's foundry support Web site at: <http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw0BSK0BNFo0At>

Magma Design Automation ==> <http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJh>

3. News

Component Library Beefs Up RF Design Suite

Ansoft and Taiyo Yuden released a device library for Ansoft Designer and Nexxim based on Taiyo Yuden's high-density miniaturized surface-mount components. The component library helps engineers designing electronic equipment (e.g., wireless local-area networks, car navigation systems, basestations, and cellular handsets) by providing accurate electrical responses and mechanical layout features for manufacturing.

The library, which consists of capacitors, ferrite beads, and multilayer inductors, is available from Taiyo Yuden's Web site. It's easy to download and configure for use within Ansoft Designer/Nexxim. This site provides Ansoft customers with the ability to search for components by name, performance data, or other specifications. Taiyo Yuden will maintain model support and upgrades, while Ansoft will address all customer support for Ansoft Designer/Nexxim.

For more information, please visit:

<http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw0BSK0BNFq0Au>

Ansoft ==> <http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw0BSK07oT0Ad>

Taiyo Yuden ==> <http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw0BSK0pcD0A>

4. News

OASIS Tools Support OpenAccess Standard

The latest version of OASIS Tooling's Mosaic developers' platform will incorporate support for version 2.2 of the OpenAccess platform. OASIS Mosaic is a development platform for semiconductor design using the OASIS interchange format and for making OASIS an extension of the OpenAccess database.

A limited timeframe, no-charge license for OASIS Mosaic still applies to OpenAccess and SEMI OASIS Working Group members.

OASIS Tooling ==> <http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw0BSK0BL2>

OpenAccess Initiative ==> <http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw>

5. News

FPGA Tool Suite Gets Makeover

Lattice Semiconductor's overhauled ispLEVER programmable-logic design tool suite improves FPGA Fmax performance by an average 22%. Also, map, place, and route runtimes are reduced by 24% for typical designs.

Enhancements in the 4.2 release include an I/O Assistant for efficient placement of mixed I/O types; the addition of new Power Calculator and ispTRACY logic-analyzer tools; a new Project Creation Wizard; major upgrades in static timing analysis, floorplanning, and DSP design; and a much faster and more fully featured ModelSim simulator from Mentor Graphics.

The ispLEVER tools support all Lattice digital programmable-logic devices. Pricing starts at \$995.

Lattice Semiconductor ==> <http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw>

6. Happenings

37th International Symposium on Microarchitecture (MICRO'04)

Doubletree Hotel, Portland, Ore.

Dec. 4-8, 2004

<http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw0BSK0BMwM0A7>

International Conference on Field Programmable Technology (ICFPT04)

The University of Queensland, St. Lucia Campus, Brisbane, Australia

Dec. 6-8, 2004

<http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw0BSK0BMwN0A8>

IP-Based SoC Design Forum and Exhibition (IP/SoC 2004)

World Trade Center, Grenoble, France

Dec. 8-9, 2004

<http://lists.planetee.com/cgi-bin3/DM/y/eiTd0DJhTw0BSK0BMwO0AA>

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