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VSI Alliance releases Soft-IP Tagging Standard

- **Tracks Soft IP information throughout design and development**
- **Fully compatible with VSIA's recently released hard-IP tagging standard**

Aptos, CA. – November 1, 2004 – The VSI Alliance (VSIA) today announced the release of the “Virtual Component Identification Soft IP Tagging Standard Version 1.0” (IPP 4 1.0) to the VSIA general membership. Complementary to, and compatible with, the VSIA’s hard IP tagging standard, “Virtual Component Identification Physical Tagging Standard” (IPP 1 2.0), announced in July 2004, IPP 4 1.0 provides a means of retaining information about an IP Virtual Component (VC) all the way through the chip design process, from source code to the GDS II physical database.

“One of the shortcomings to IP-based chip design has been the lack of a method for tracking the history of the design development of a piece of IP during chip design,” said Ian Mackintosh, Board of Directors VSIA, and President of OCP-IP. “VSIA’s soft- and hard-IP tagging standards give IC developers the means of tracking important IP information, including source, version, date and IP provider.”

“VSIA’s soft-IP tagging standard allows important chip specifications and information to be monitored and shared throughout the design and manufacturing process,” said Ken Goodnow, senior engineer, IP Core Development at IBM. “The tagging methods described in the standard

also offer VC users and providers the ability to accumulate Soft IP information at the chip GDS II level to help ensure the quality of the final chip design”

The soft IP tagging standard takes identification information from the IP source file and provides a process for passing this information through each chip-level design step, including synthesis, timing, placement, wiring and other steps leading to the chip's GDS II generation. This information can include identification, vendor ID, and, most importantly version information, allowing a chip designer to explicitly identify the version of a piece of soft IP even after it has been absorbed in the overall "sea of gates" of the chip. IC designers, semiconductor foundries, VC providers, and EDA tool manufacturers can use the methods in the standard to track identification information throughout each level of the chip-development process. At each level, tracking information is obtained from the previous level and is transported to the next level using the appropriate output format; this makes the information independent of the design methodology, design tools and EDA provider.

Foundries can use the standard to provide additional services to support a quality check prior to IC manufacturing. VC providers can use the standard to include version, date, and source information that is useful for quality and business purposes. EDA tool vendors can use the standard to transport VC information from one stage of a toolset to the next, from an industry-standard format into a toolset, and in the output of an industry-standard format at the end of the tool chaining. They can also provide new software to collect, correlate and display this information at convenient places in the tool chain.

Either directly or through a tool, VC users can view information about the VCs included in a chip and the steps the IP went through in the chip's development process. Thus, developers can easily determine the specific version of a particular piece of IP at any phase of the design flow, and readily confirm the correctness of that version contained in the chip.

About the VSIA IP Protection Pillar

The IP Protection Pillar (IPP) defines, documents, and demonstrates open, interoperable, standards-based solutions and promotes awareness of IP protection schemes and practices that

balance the necessary level of security with customer usability of IP to foster the proliferation of design reuse. Participants in the IPP Pillar include: IBM, Cadence Design Systems, Freescale Semiconductor, Intel, Mentor Graphics, ST Microelectronics, Sonics and Taiwan Semiconductor Manufacturing Company Ltd. (TSMC).

For more information on the VSIA and the Pillars, go to www.vsi.org

About VSIA

The VSI Alliance (VSIA) is an open, international organization that includes representatives from all segments of the SoC industry: System houses, Semiconductor vendors, Electronic Design Automation (EDA) companies, and Intellectual Property (IP) providers. VSIA's mission is to dramatically enhance the productivity of the SoC design community by providing leading edge commercial and technical solutions and insight into the development, integration and reuse of IP. VSIA has wide industry participation with more than 70 member companies from around the world. Membership is open to any company with an interest in the development and promotion of business solutions and open standards used in the design of System-on-Chip. For more information, visit the VSIA web site at www.vsi.org, or e-mail to info@vsi.org.

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