



MIPS TECHNOLOGIES INTRODUCES NEW SYSTEM CONTROLLER FOR 24K™ CORE FAMILY

SOC-it™ OCP System Controller Increases System Performance, Reduces Costs and Time-to-Market of SOCs Using Highest-Performance MIPS32® 24K™ Processor Cores

MOUNTAIN VIEW, Calif., — August 16, 2004 — MIPS Technologies, Inc. (NASDAQ: MIPS), a leading provider of industry-standard processor architectures and cores for digital consumer and business applications, today introduced a new SOC-it™ OCP system controller optimized for the MIPS32® 24K™ core family, which enables SOC designers to dramatically increase overall system performance when compared to competitive offerings. The result is a complete system-level solution that offers up to 100 percent memory bandwidth efficiency and very low subsystem memory latency.

The SOC-it OCP system controller seamlessly connects to a 24K core and is MIPS Technologies' latest addition to its SOC-it family. It features a tightly coupled memory controller and multiple, high bandwidth, dual-port interfaces to intellectual property (IP) blocks. Using the SOC-it OCP system controller, designers also can reduce development time by using modular bridges to industry-standard buses.

“SOC designers who need to keep costs down while adding more features and functionality to demanding consumer applications have an ideal solution in an optimized system controller for our high performance 24K cores,” said Russ Bell, vice president of marketing at MIPS Technologies. “The SOC-it OCP controller offers a highly flexible, cost-effective means for moving massive amounts of data through an SOC at very high speeds. The challenges of increasingly complex SOC design demand standard buses and interfaces, and OCP is helping to make plug-and-play SOC design a reality.”

“Standard interconnect interfaces are critical in meeting the challenges of increasingly complex SOC design and shrinking market windows. We are delighted to have OCP featured as the native interface in MIPS Technologies' new system controller for the 24K core family,” said Ian Mackintosh, president of OCP-IP.

About the SOC-it Controller Family

Modular, flexible and scalable SOC-it system controllers make it easy to meet the needs of higher performance, next-generation applications. Features include:

- An integrated memory controller that is optimized for, and closely coupled with, the MIPS CPU core in SOC designs. It supports industry-standard DRAM interfaces to deliver up to 100 percent memory bandwidth efficiency and latency as low as 8-1-1-1 system clocks.
- Dual-port IP interfaces and point-to-point switched bus interconnects. This offers a significant performance advantage over a shared bus architecture by enabling the CPU to access a device while another peripheral simultaneously accesses the SDRAM through the memory controller.
- Support for vectored interrupts with software examples for interrupt handlers to speed software development.

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- The flexibility of a memory arbiter that can be modified to prioritize data packets.
- Full compliance to industry-standard buses to preserve existing IP blocks.
- A fully static design that enables low-power operation to extend battery life in portable applications.

About the MIPS32 24K Family

The MIPS32 24K core family, which includes the 24Kc™, 24Kc Pro, 24Kf™ and 24Kf Pro versions, offers performance up to 625 MHz worst case in a 0.13 micron process, the highest frequency available in 32-bit synthesizable cores for embedded markets, while minimizing design time and reducing product costs. Tailored SOC design methodologies, an OCP interconnect structure, standard libraries and on-chip memories from industry-leading companies help speed time-to-market, an important advantage for a processor core suited to consumer applications such as digital and interactive TVs, set-top boxes and DVD players.

The 24K family is the first in the embedded industry to use the OCP standard as a native interface. The OCP standard facilitates plug-and-play SOC design and helps customers exploit the new core family's advanced architectural features; reduce development time and lower overall design costs. Designers who use the 24K core can reuse OCP-compliant cores across multiple MIPS-Based™ SOCs. OCP also eliminates the need to repeatedly modify the core and preserves the verification and test benches by defining all of the core's natural interface capabilities in a standardized way. These interface definitions enable third-party verification IP and tools to transparently adjust to the precise requirements of each IP.

About OCP-IP

The OCP International Partnership Association, Inc. (OCP-IP) was announced in December 2001 to promote and support the open core protocol (OCP) as the complete socket standard that ensures rapid creation and integration of interoperable virtual components. OCP-IP's Governing Steering Committee participants are: Nokia, Texas Instruments, STMicroelectronics, United Microelectronics Corporation, Toshiba Semiconductor Group (including Toshiba America TAEC), Sonics and other industry leading companies. OCP-IP is a non-profit corporation delivering the first fully supported, openly licensed core-centric protocol that comprehensively fulfills system-level integration requirements. The OCP facilitates IP core reusability and reduces design time and risk, along with manufacturing costs for SOC designs. VSIA endorses the OCP socket, and OCP-IP is an Adoption Group of the VSI Alliance. For additional background and membership information, visit www.ocpip.org.

About MIPS Technologies

MIPS Technologies, Inc. is a leading provider of industry-standard processor architectures and cores for digital consumer and business applications. The company drives the broadest architectural alliance that is delivering 32- and 64-bit embedded RISC solutions. The company licenses its intellectual property to semiconductor companies, ASIC developers and system OEMs. MIPS Technologies and its licensees offer the widest range of robust, scalable processors in standard, custom, semi-custom and application-specific products. The company is based in Mountain View, Calif., and can be reached at +1 (650) 567-5000 or www.mips.com.

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