



VLSI Design and Education Center Joins OCP-IP

PORTLAND, Ore. — May 17, 2005 — Open Core Protocol International Partnership (OCP-IP) today announced that the VLSI Design and Education Center (VDEC), has joined the organization. VDEC, established in 1996, is headquartered in the University of Tokyo and serves academia throughout Japan.

As an intellectual education and research center on VLSI (Very Large Scale Integration) technology, VDEC's mission is to educate students and provide support on VLSI chip fabrication for all academic organizations throughout Japan.

VDEC performs various kinds of activities including exchange of VLSI design information as IPs, and provision of CAD software and licenses supporting chip design and fabrication.

Several different VLSI fabrication technologies, various popular CAD software supporting Verilog /HDL/VHDL/C simulation, synthesis, layout design and verification for digital/analog VLSIs, and measurement and testing facilities are provided through VDEC. Over 450 research groups from over 150 universities in Japan are utilizing the services and support of VDEC. Many software licenses are issued through VDEC via nine branches in Japan.

The addition of VDEC to the membership roster adds to the tremendous support that OCP-IP has already enjoyed throughout Japan and the rest of Asia. Other OCP-IP Japanese members include: Semiconductor Technology Academic Research Center (STARC), FueTrek, Yamaha, Kawasaki, Zuken, SIPAC, Governing Steering Committee member, Toshiba, and several leading universities.

“We are very excited to participate in OCP-IP. As hundreds of chips are fabricated each year at VDEC, it is extremely important that we have a standardized on-chip bus interface. It makes it much easier to realize IP macro exchange among various VDEC users,” said Masahiro Fujita Professor, VLSI Design and Education Center

OCP-IP members receive free training, support, software tools, and documentation. This infrastructure allows IP and EDA vendors to eliminate the need to internally design, document, train and evolve a proprietary standard and set of support tools. This enables IP and EDA vendors to focus their efforts and resources on the challenges of developing IP that can be quickly integrated and easily verified in a wide variety of SoC designs. As a result, IC design teams can dedicate their critical resources to the design and delivery of products.

“We have seen tremendous support throughout Japan,” said Ian Mackintosh, president OCP-IP. “Our relationship with VDEC will facilitate further collaboration with the country's universities, and help us communicate to our membership and so better serve industry interests.”

About OCP-IP

The OCP International Partnership Association, Inc. (OCP-IP) formed in 2001, promotes and supports the Open Core Protocol (OCP) as the complete socket standard ensuring rapid creation and integration of interoperable virtual components. OCP-IP's Governing Steering Committee participants are: Nokia [NYSE: NOK], Texas Instruments [NYSE: TXN], STMicroelectronics [NYSE: STM], Toshiba Semiconductor Group (including Toshiba America TAEC), and Sonics. OCP-IP is a non-profit corporation delivering the first fully supported, openly licensed, core-centric protocol comprehensively fulfilling system-level integration requirements. The OCP facilitates IP core reusability and reduces design time, risk, and manufacturing costs for SoC designs. VSIA endorses the OCP socket, and OCP-IP is affiliated with the VSI Alliance. For additional background and membership information, visit www.OCP-IP.org.

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