



ARTERIS SA JOINS OCP-IP

PORTLAND, Ore— April 4, 2006 — Open Core Protocol International Partnership (OCP-IP) announces that Arteris S.A. has joined the Organization. Arteris is a leading provider of Network-on-Chip (NoC) solutions for on-chip communications challenges by delivering intellectual property, associated design tools and design services for integration of complex SoCs. Joining OCP-IP allows Arteris to support the vast multitude of designers utilizing the benefits of OCP in their designs to enable IP reuse and shorten time to market.

Arteris Network-on-Chip architecture relies on a flexible topology of switches and links transporting data packets between Network Interface Units (NIUs), with each NIU connecting to an IP core using a specific socket protocol. This structure allows seamless connection of IPs using various protocols, data widths and clock rates to the same Network-on-Chip, thereby enabling true IP reuse. Arteris has already announced support for other popular IP interfaces, with validated Network Interface Units, and has developed customized NIUs supporting proprietary customer protocols.

“Arteris packet-based Network-on-Chip architecture is a natural match for many of the OCP 2.1 features, and using our NIU approach to connect OCP-compliant cores such as processors, DMAs, memories, and other specialized interfaces is very efficient in terms of system-level performance and silicon cost.” said Philippe Martin, Product Marketing Director at Arteris. “By joining OCP-IP and widening the range of interface protocol supported, Arteris is well positioned to provide interconnect solutions to SoC designers that have adopted OCP as part of their IP reuse strategy, but also need to integrate IP cores supporting legacy and proprietary interfaces.”

“Network on Chip addresses many demanding challenges resulting from the huge complexity of silicon systems. These challenges make reuse more critical than ever,” said Ian Mackintosh, president OCP-IP. “OCP enables reuse regardless of chip architecture, interconnect approach or processor cores featured. We are pleased to see Arteris adopt and support OCP.”

OCP-IP members receive free training, support, software tools, working group products and documentation. This infrastructure allows IP and EDA vendors to eliminate the need to internally design, document, train and evolve a proprietary standard and set of support tools. This enables vendors to focus their efforts and resources on the challenges of developing IP that can be quickly integrated and easily verified in a wide variety of SoC designs. As a result, IC design teams can better focus on their core competencies and dedicate their critical resources to the design and delivery of products.

About OCP-IP

The OCP International Partnership Association, Inc. (OCP-IP), formed in 2001, promotes and supports the Open Core Protocol (OCP) as the complete socket standard ensuring rapid creation and integration of interoperable virtual components. OCP-IP's Governing Steering Committee participants include: Nokia [NYSE: NOK], Texas Instruments [NYSE: TXN], Toshiba Semiconductor Group (including Toshiba America TAEC), and Sonics. OCP-IP is a non-profit corporation delivering the first fully supported, openly licensed, core-centric protocol comprehensively fulfilling system-level integration requirements. The OCP facilitates IP core reusability and reduces design time, risk, and manufacturing costs for SoC designs. VSIA

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endorses the OCP socket, and OCP-IP is affiliated with the VSI Alliance. For additional background and membership information, visit www.OCP-IP.org.

About Arteris

Arteris, SA, provides Network on Chip solutions to transport and manage the on-chip communications within complex System-on-Chip (SoC) integrated circuits, increasing performance, reducing number of global wires, with lower power utilization while enabling the most complex, IP-laden designs. It allows chip developers to implement efficient and high-performance Network-on-Chip (NoC) designs, overcoming limitations of traditional layered or pipelined bus-based architectures. Arteris' technology is scaleable in terms of the number of IP blocks designers can network, as well as with deep submicron silicon manufacturing processes. The NoC solutions are compatible with existing design flows and with IP interface standards. The Paris-based company operates globally with offices in Boston and San Jose, California. Arteris has raised more than \$12 million in equity investment from an international set of venture capitalists, including Crescendo Ventures, Techno Venture Management and Ventech. More information can be found at www.arteris.com.

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