



## **OCP-IP Announces Availability of New Debug White Paper**

*New OCP White Paper Discusses Hardware, Software and Mixed SoC Prototyping*

**BEAVERTON, Ore. — April 03, 2007** — OCP-IP today announced the availability of a white paper discussing an approach to a standardized OCP-bus compliant debug interface. The proposed debug solution is an optional OCP port, implementing a Debug Interface Socket, which can be added to all cores and IP blocks to support a more uniform method of on-chip system analysis and access to embedded information at the core, multicore, and systems levels. The debug interface socket defines several layers of extended functionality to address the diverse and increasing debug needs for software, hardware, and mixed SoC prototyping and is intended to be compatible with other industry standards efforts addressing debug and related on-chip issues.

Work on the white paper was completed by the OCP-IP Debug Working Group led by Texas Instruments, MIPS Technologies, and Pixelworks.

The document describes an overall debugging framework as the base of the OCP debug interface. In the same way that the OCP data framework is a functional superset for various bus interfaces and data structures, the OCP Debug Framework defines an OCP Debug Interface Socket that can connect to a superset of debug solutions, including those developed outside of OCP-IP. The paper loosely defines requirements and a set of debug signals at the OCP Socket and fabric levels, which will be finalized later in 2007 after more testing and prototyping, but leaves much of the specific options for implementation open to IP and tools vendors.

Commercial and licensable instrumentation IP and tools supporting many of the Debug Socket Interface options are available today from OCP-IP members.

“Complex SoC adds new requirements and challenges in terms of increasing visibility and debug control to a system, and standardizing integration of hardware and software instrumentation into design flows, and supporting emerging needs for architectures incorporating complex network on chip buses, multiple cores, multithreading, embedded security, power management and other issues are required,” said Ian Mackintosh, president and chairman of OCP-IP. “One goal of the white paper is to open discussion on emerging needs in SoC design that enables companies to offer a library of proven instrumentation IP blocks and tools that address more complex debug situations and purposes as part of the vast and ever expanding OCP infrastructure available to our members.”

Companies wishing to participate in the OCP-IP Debug Working Group are invited to contact [admin@ocpip.org](mailto:admin@ocpip.org)

To download a copy of the debug white paper, visit [http://www.ocpip.org/socket/whitepapers/OCP-IP\\_Debug\\_Working\\_Group\\_Whitepaper\\_3\\_26\\_2007.pdf](http://www.ocpip.org/socket/whitepapers/OCP-IP_Debug_Working_Group_Whitepaper_3_26_2007.pdf)

### **About OCP-IP**

The OCP International Partnership Association, Inc. (OCP-IP), formed in 2001, promotes and supports the Open Core Protocol (OCP) as the complete socket standard ensuring rapid creation and integration of interoperable virtual components. OCP-IP's Governing Steering Committee participants include: Nokia [NYSE: NOK], Texas Instruments [NYSE: TXN], Toshiba Semiconductor Group (including Toshiba America TAEC), and Sonics. OCP-IP is a non-profit corporation delivering the first fully supported, openly licensed, core-centric protocol comprehensively fulfilling system-level

integration requirements. The OCP facilitates IP core reusability and reduces design time, risk, and manufacturing costs for SoC designs. VSIA endorses the OCP socket, and OCP-IP is affiliated with VSIA. For additional background and membership information, visit [www.OCPIP.org](http://www.OCPIP.org).

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