

Single Flow for Interconnecting OCP-based IP and Auto-generating Design Views

The latest challenge facing SoC teams is the construction of a design flow that seamlessly combines:

- A complex central Interconnect Matrix
- Auto generation of a diverse range of system design views

While, suppliers of Interconnect Matrix components provide complex architectures for hardware, the SoC team is also responsible for producing other associated design view outputs such as documentation and code for software development, test and verification.

Ultimately the team is responsible for delivering a fully tested, documented and usable product – on time.

In this article, we outline a flow, based around Beach Solutions® software, which results in seamless interoperability between disparate tools and methods.

Central Interconnect Matrix

A central Interconnect Matrix allows a designer to create multiple memory maps and control communications paths based on specific master and slave combinations easily and quickly.

The design and creation of an Interconnect Matrix component is well defined and tools providing suitable architectures are available, from companies such as Sonics.

Auto design view generation

SoC design teams now realize the benefits of storing register address map information in a central repository and use auto-generation techniques to create a diverse range of design views for software developers, hardware designers, verification engineers and documentation teams. Initiatives such as SPIRIT (IP-XACT) and software companies like Beach Solutions provide out-of-the-box solutions for the capture of IP and system interface information (in a generic form) and the auto-generation of design views.

The breadth of designs views that can be generated depends upon the depth of information that is captured and stored.

Beach Solutions advocate that, in addition to other attributes, there are 3 essential elements to capturing interface information for maximum auto-generation purposes:

1. **Physical interfaces:** discrete ports, point-to-point signals and connections
2. **Physical memory map:** register, bitfield and memory definitions
3. **Transaction level:** base addresses for located IP and allowable initiator/slave communications

The Beach Solutions generic flow is based on a three-step methodology: capture, validate and auto-generate a broad range of design views.

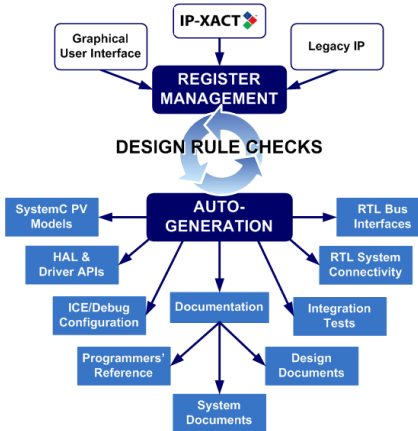
Interconnect Matrix – more than a black box

The architecture of an Interconnect Matrix is typically hidden from the SoC designer – indeed this is one of its advantages. Unfortunately, this means that for auto-generation purposes an Interconnect Matrix is typically captured as an IP core with just physical interface information, i.e. only one of the essential elements.

This means that you effectively have a black box IP core in your system, to which other cores are physically connected, from which you need to auto-generate a complete set of system views.

The physical interface information permits auto-generation of some hardware outputs (such as RTL representation of system connectivity), but precludes most software and verification views.

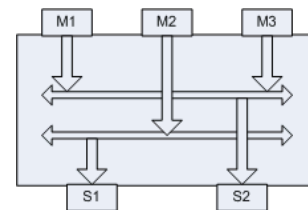
The success of a design flow incorporating auto generation tools depends upon capturing the minimum amount of information that will permit generation of the maximum number of different design view. So the solution to incorporating an Interconnect Matrix component into such a flow is to treat it as a ‘grey’ rather than a black box.



Interconnect Matrix – a grey box...

For a scaleable and generic solution, the Interconnect Matrix component should be viewed as grey box. This means that when one or more such components are instanced in a system, visibility of the transaction-level communication paths through them is known.

Using Beach Solutions EASI Tools as an example, an Interconnect Matrix is captured as an EASI database ‘System’ object (similar to IP-XACT component). For example, an interconnect that allows Master M1 and M3 to access S2 but Master M2 can only access S2.



IP core representation

Other IP cores are captured as EASI database ‘IP Block’ objects, each having a corresponding transaction interface(s) to the Interconnect Matrix component. Information about memory mapped registers, bitfields and memories is captured within each IP Block.

System representation

The System object in the EASI database is also used to represent the top-level of the final system. Each system can contain:

- Instantiations of components
- Transaction-level communication paths
- Point-to-point connections

Maintaining these levels of information in the captured data means that the 3 essential requirements for maximum auto-generation have been met and hence generation of a broad range of design views becomes possible.

Proposed design flow

The proposed iterative design flow that allows for auto-generation of multiple design views for a system with a complex OCP Interconnect Matrix uses tools readily available from commercial tool vendors.

1. Auto create Interconnect block

Use a graphical wizard and sophisticated GUI, available in EASI Tools, to capture the Interconnect Matrix component as a system with physical ports, parameters and transaction level communication paths. The wizard can be pre-configured with master and slave interface types (for example OCP) together with any associated interface constraints (parameters).

2: Auto-generate Interconnect description

Using EASI Tools, auto-generate documentation describing the Interconnect Matrix component. This can be supplied to a vendor (such as Sonics) as a requirement specification for an Interconnect Matrix architecture. Alternatively other custom views can be generated that interface directly with tools that produce RTL descriptions of matrix architectures.

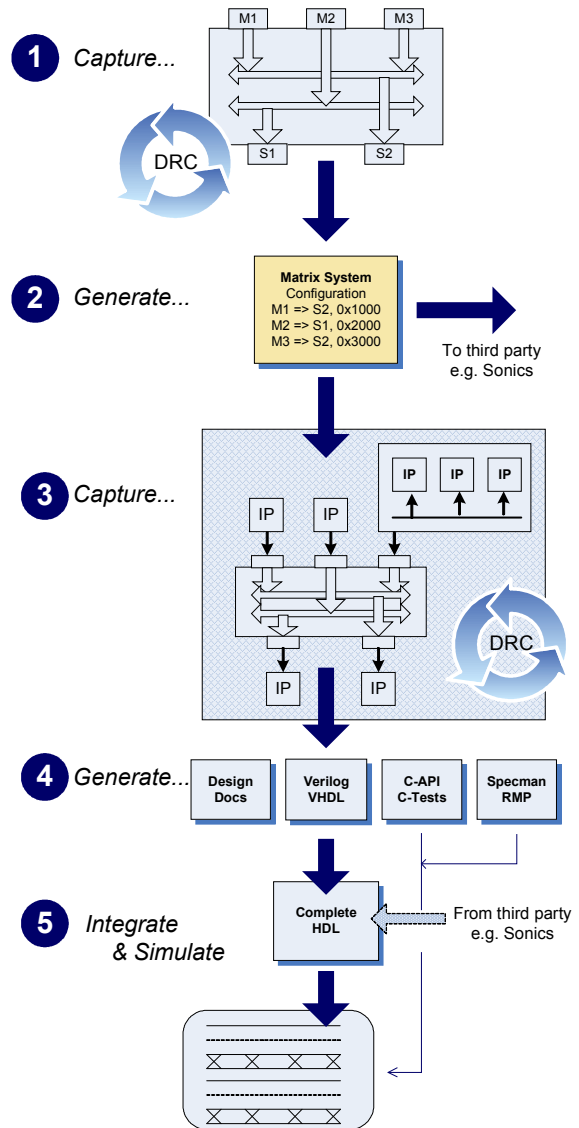
3: Capture final System description

A System is captured in the EASI central repository containing an instance of the Interconnect Matrix component, other IP and the transaction-level communication paths between the IP and the Interconnect Matrix. At this stage, generation of software, documentation and some test views become possible.

A step further, is the capture of point-to-point connections discrete ports in the same EASI database. The final essential element required for maximum auto-generation. Beach EASI Tools provide clever automated graphical utilities for connecting ports together using a single 'click'. These include:

- Auto connecting bus signals with a single click
- Auto connecting ports based on name or alias
- Auto connect ports based on their type

The final system and its interconnections is data checked against in-built and user-defined rules.



4: Auto-generate all views

Once checked, the data is used as a reliable source for the automatic generation of design files for use by all members of a development team. This is now possible because the complete path from the top-level system down through the Interconnect matrix to individual registers and bitfields is captured in the central EASI database (remember the 3 essential elements).

5: Integrate Matrix architecture

Receive the matrix architecture (HDL) from a third party or internal source and include this in the generated system HDL to create a complete system description.

As a bonus, the captured information in the final EASI system database allows for a system level RTL connectivity view to be created, this contains declarations and fully connected instantiations for all IP in the final system, including the matrix component i.e. the RTL description contains fully interconnected 'sockets'.

The supplied matrix architecture is simply referenced by the generated connectivity RTL i.e. it is inserted into the matrix socket. RTL descriptions for the architectures of the other IP Cores are also referenced to create a full model for simulation.

Summary

This article has highlighted the challenges associated with using a complex Interconnect Matrix component in a SoC design flow that utilizes auto generation techniques to shorten project cycles.

Used by leading semiconductor vendors in mobile, consumer electronics and communications markets, Beach Solutions EASI Tools Suite auto-generates the hardware, firmware, verification configuration files and documentation necessary to package IP and integrate platform-SoCs while managing data and deliverables for the hardware and software teams as the design, requirements and specification evolve.