



Platform Architecture Design

*OCP-IP Pavilion at DATE
March 2008*

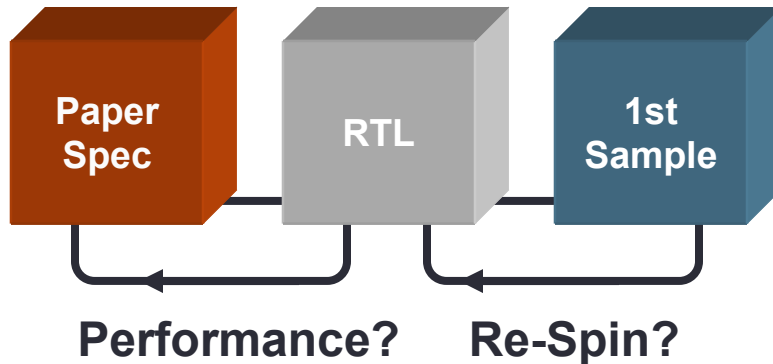
Today's Reality

- 38% cite system architecture design and specification as the highest cause of schedule delays
- Quickly followed by system integration, test and software development (all above 25%)
- In 2007 the cost of software development for an SoC surpassed the cost of IC design

Single application system	➤	Multi application system
Local memory sub-systems	➤	Complex memory hierarchy
Local, shared bus	➤	Intelligent interconnects (NoC)
Single processor IP	➤	Multi-Processor/Core & Interconnect IP
"Single" SW stack	➤	Multiple, dependent SW stacks

Source: VDC and Gary Smith EDA 2007

The Breakdown of Traditional RTL Methods

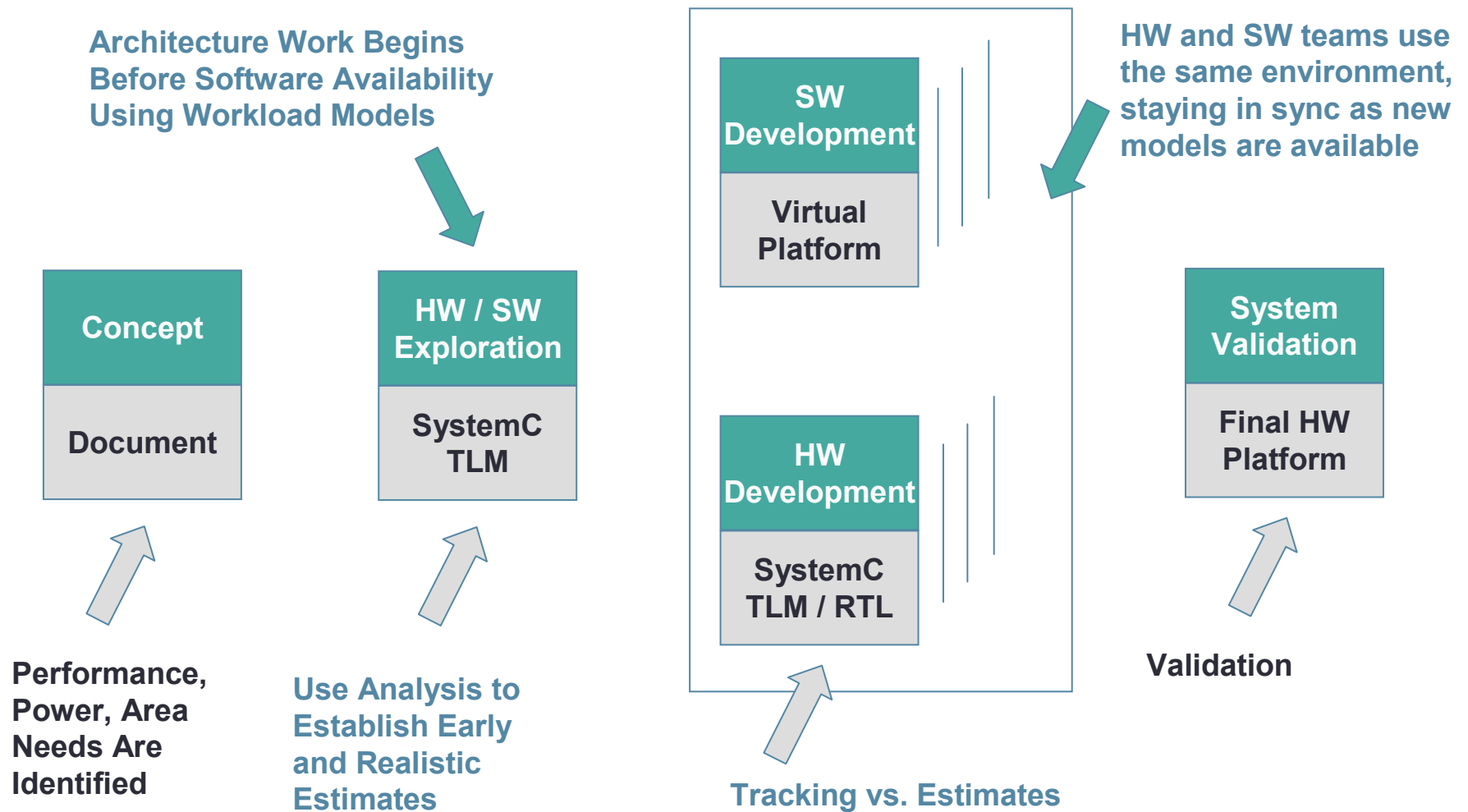


- No visibility into global interconnect/memory subsystem performance throughput
- No HW-SW validation of global interconnect/memory subsystem performance throughput
- Slow, inefficient verification of new RTL IP/Subsystems in the system

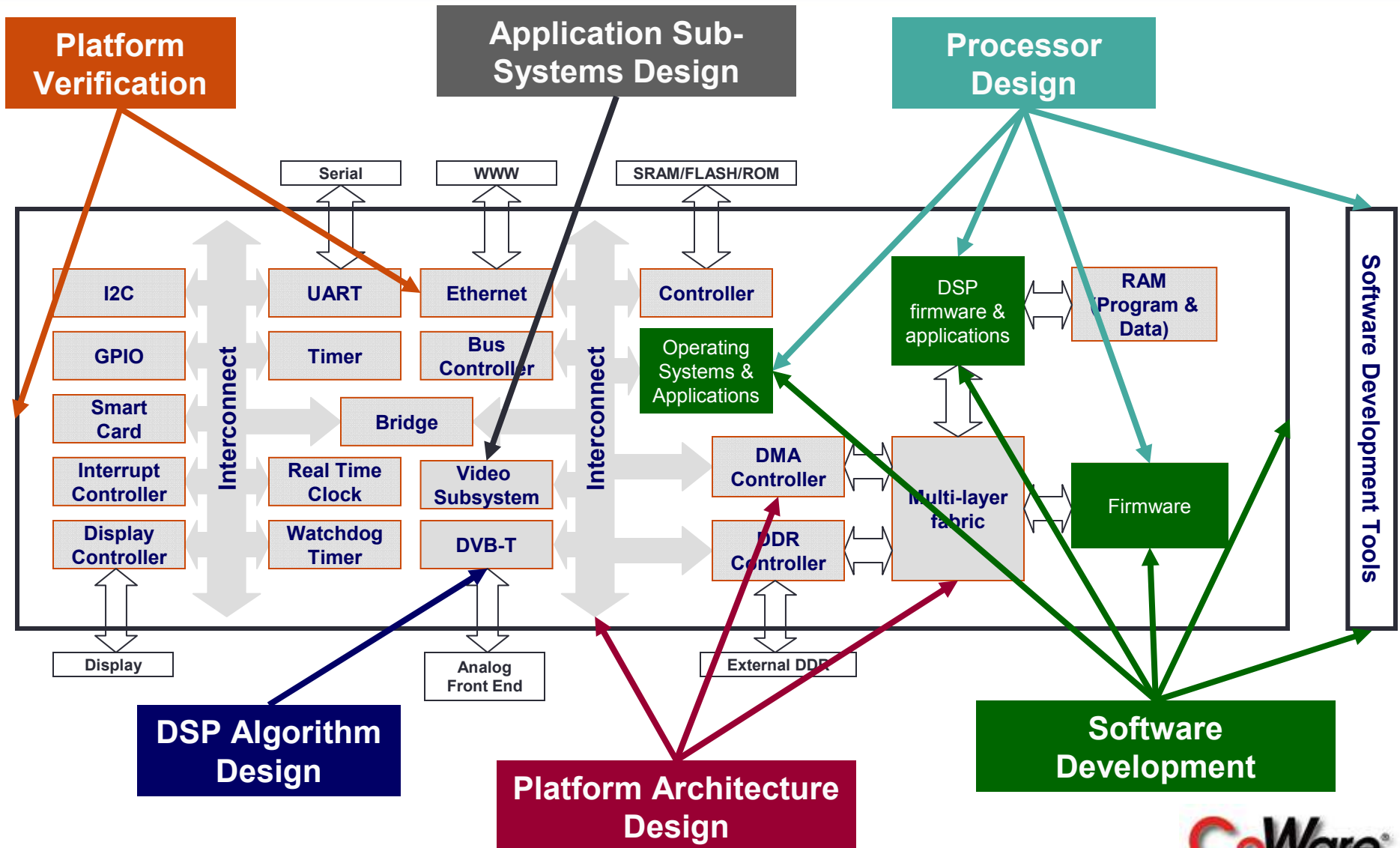
What is Needed from ESL Methods?

Measurable improvement in product performance & cost
Improved verification productivity and product quality
Cycle time reduction over traditional RTL methods

Designing the Best Architecture

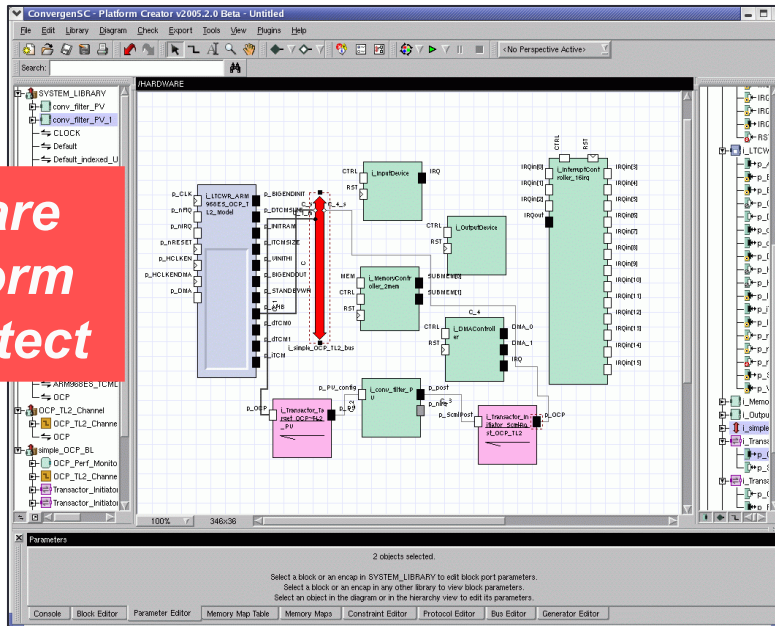


CoWare ESL 2.0 Solutions



CoWare Platform Architect

CoWare
Platform
Architect



SystemC Platform
Capture and Analysis

SystemC IP Model
Development and Debug

SystemC
TLM & SCML

CoWare
Model
Library

CoWare
Model
Designer

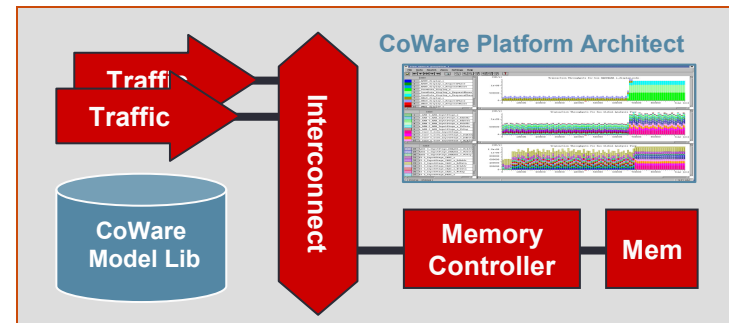
```
#include "system.h"
#include "scv.h"
#include "scot/record/cwvrecord.h"
sc_trace_file *tf;
#include <set>
#include <math.h>
#define USER_SCV
// example packet structure
enum packet_type {
    Packet_read, Packet_write
};
};
```

Channel	Value
clk	0
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Platform Architecture Design Solutions

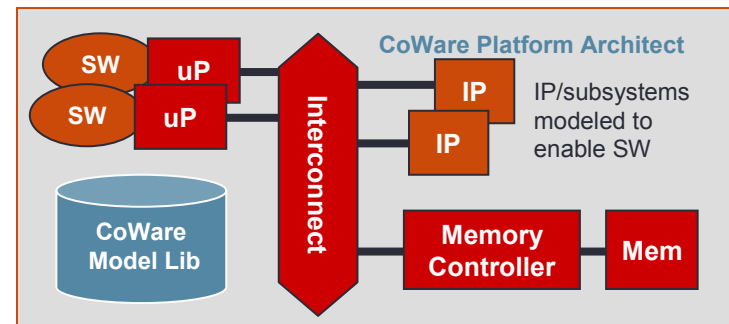
- Interconnect / Memory Subsystem Performance Optimization and Validation using Traffic Generation

Early and Accurate Estimates



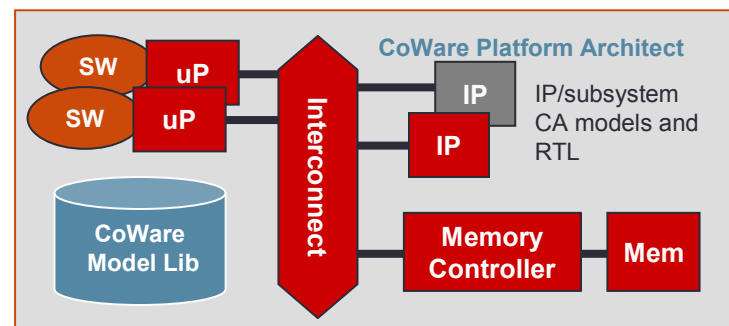
- Interconnect / Memory Subsystem Performance Optimization and Validation using CA Processor Models and Software

Product Validation Before RTL

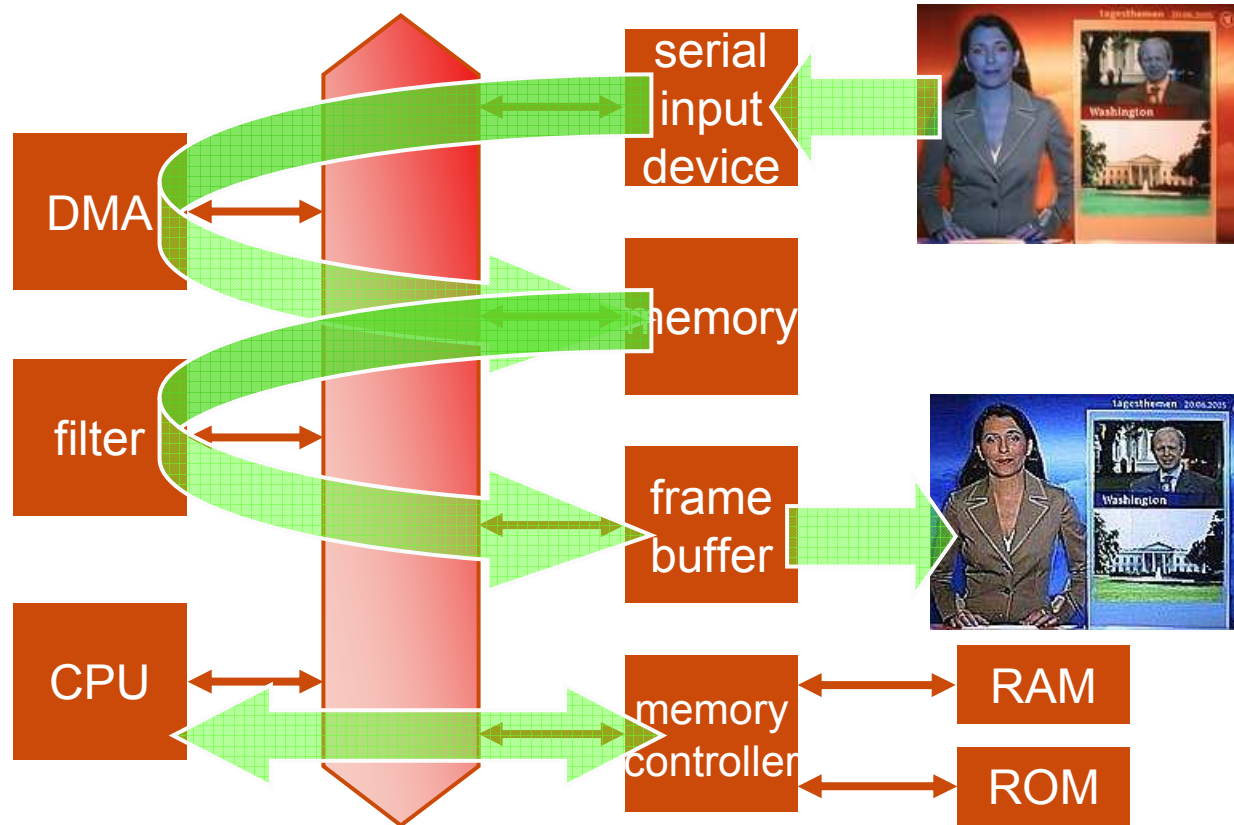


- Platform-level Debug and Performance Benchmarking of Integrated IP/Application Subsystems

Golden Reference for RTL

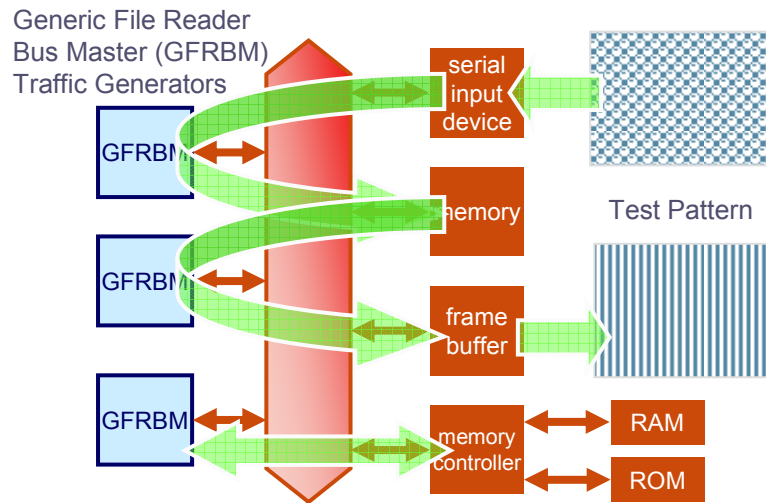


Example: DTV Video Processing Subsystem

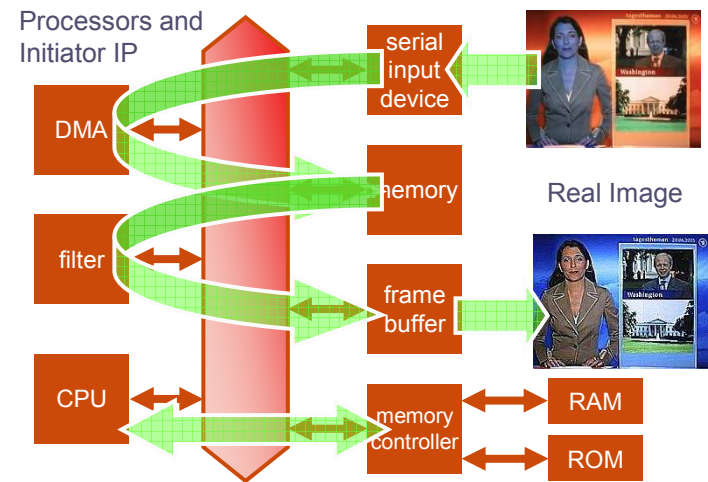


Convolution Filter Application

Analysis Scenarios



**Convolution Filter Application
Using Transaction Workload Models**



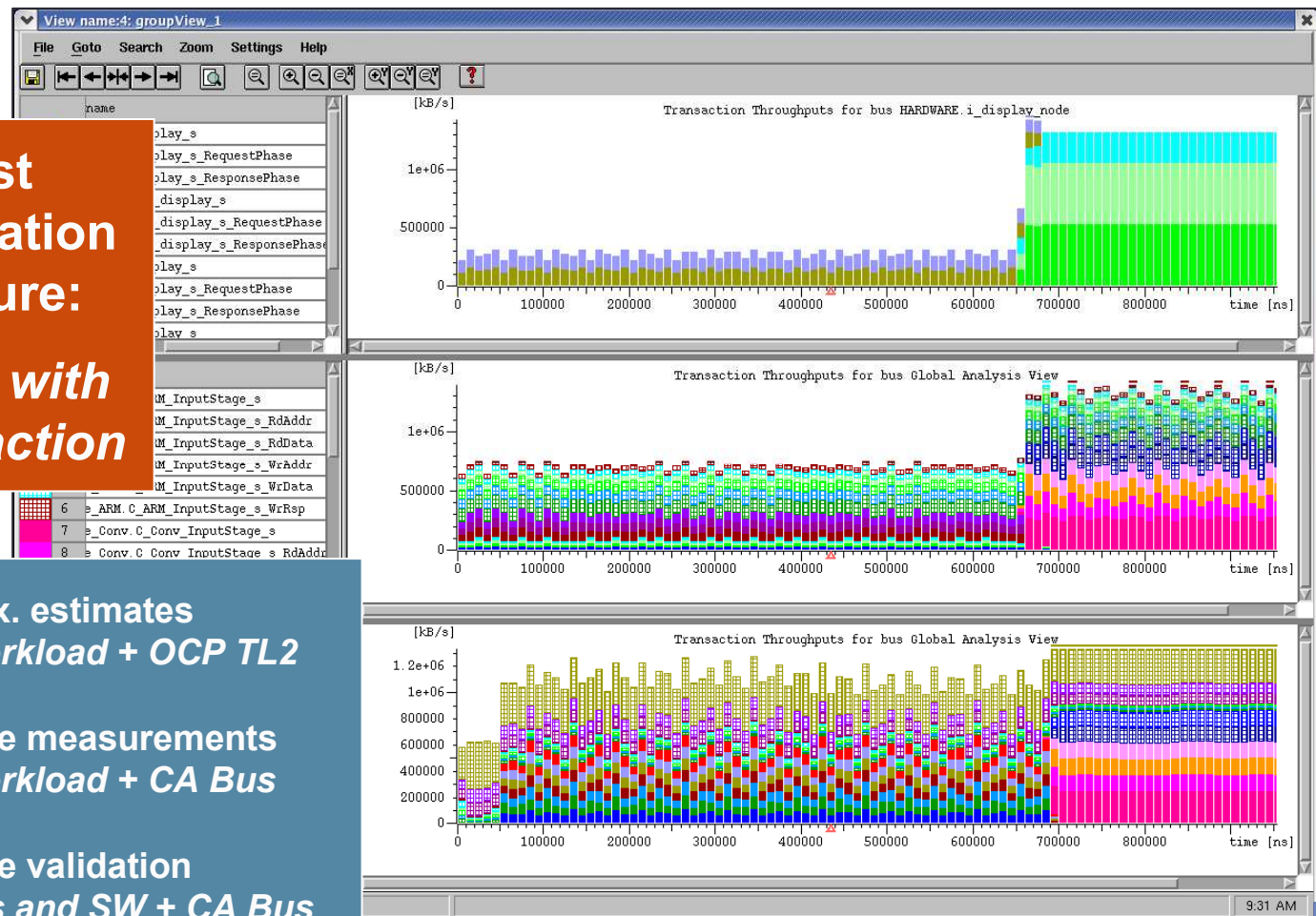
**Convolution Filter Application
Using Processors and Software**

- 1. Traffic generation, no SW**
Timing approximate estimations
- 2. Optimize interconnect**
Cycle-accurate measurement
- 3. Add processors, models, & SW**
Cycle-accurate HW/SW validation
- 4. Reuse for speed optimized VP**
Instruction-accurate SW development

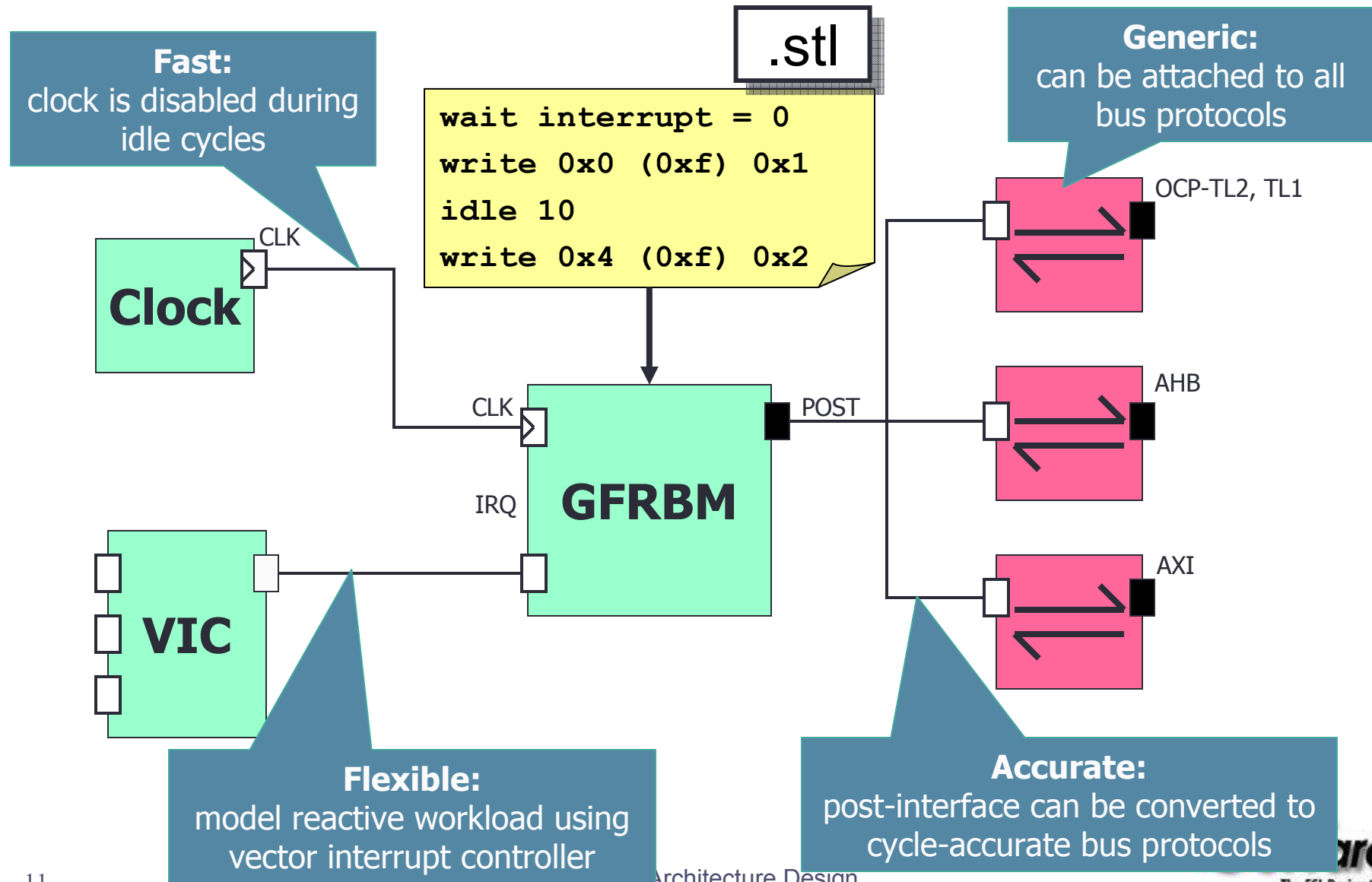
Analysis Tracking vs. Estimates Measurable and Deterministic Results

**The Best
Communication
Architecture:
*Multi-layer with
Split-transaction***

- Timing approx. estimates
GFRBM workload + OCP TL2
- Cycle accurate measurements
GFRBM workload + CA Bus
- Cycle accurate validation
Processors and SW + CA Bus



Traffic Generation with the Generic File Reader Bus Master (GFRBM)



GFRBM Accuracy

- GFRBM can generate cycle accurate traffic
 - Powerful Socket Transaction Language (STL)
 - Connects to CoWare SCML Post transactors which translate posted transactions into cycle-accurate bus traffic
- Accuracy depends on characterization of the workload
- Accuracy can be validated against reference



- Timing approx. estimates
GFRBM workload + OCP TL2
- Cycle accurate measurements
GFRBM workload + CA BL
- Cycle accurate validation
Processors and SW + CA BL

Getting Started – How CoWare Helps

■ IP Model Availability

- CoWare Model Library – ISS and Interconnect IP Models
- Generic IP Library – including Traffic Generation
- Starter Kit example platforms

■ Ease of Modeling

- SystemC component wizard
- Standards-based SCML reuse methodology
- Carbon Model Studio for RTL reuse

■ ESL Expertise and Consulting

- C++, SystemC, and TLM language training
- Methodology consulting and modeling services
- Tool technology and methodology integration

Designing the Best Architecture

- **ESL enables better product performance through:**
 - Interconnect modeling and optimization
 - Architecture performance measurement & validation
 - Development of architecture-matched algorithms, software, and processors
- **ESL enables lower product power consumption through:**
 - Design optimization
 - Avoid over-design at the product definition stage
 - Using custom (application-specific) processors
- **ESL impact on the product lifecycle:**
 - Increase market share and command higher prices
 - Product validation prior to costly implementation
 - Reduce product development schedule, cost, and risk

CoWare[®]
The ESL Design Leader



Software



Systems on Chip



Devices