

The Complete OCP Compliance Environment

CoreCreator® provides a single graphical or command line based environment for validating Open Core Protocol (OCP) implementations and “componentizing” OCP compatible cores. CoreCreator streamlines the generation and packaging of core models, interfaces, timing parameters, synthesis scripts, test vectors, and verification suites necessary for efficient IP core reuse and SoC integration.

Validation and componentization is accomplished through three systematized tasks: (1) validate the OCP implementation, (2) capture the relevant core representations, and (3) package the core for reuse.

CoreCreator also provides an environment for stimulating a core (or multiple cores) and analyzing performance and functionality in a system environment. CoreCreator’s high degree of automation, featuring tight feedback loops, enables cores to be rapidly componentized to make reuse straightforward and predictable.

Key Features

Comprehensive Design Environment for Importing Existing IP Cores or Creating New IP Cores

- OCP protocol and physical constraint compliance verification
- Maximum frequency and gate area estimation

Automated Functional Verification Environment

- Highly automated environment for configuration, simulation, logic synthesis and timing analysis
- IP core traffic trace generation
- Configurable OCP behavioral models for core validation independent of a full system implementation
- OCP behavioral models can be controlled using Verilog Task Interface
- User-defined (non-OCP) core interface support
- TCL-scripting for auto-generation of configuration files and timing constraints

IP Core Packaging for Plug-and-Play Integration

- Physical constraint extractor and packager
- Packager for all necessary verification files including scan test and functional vectors

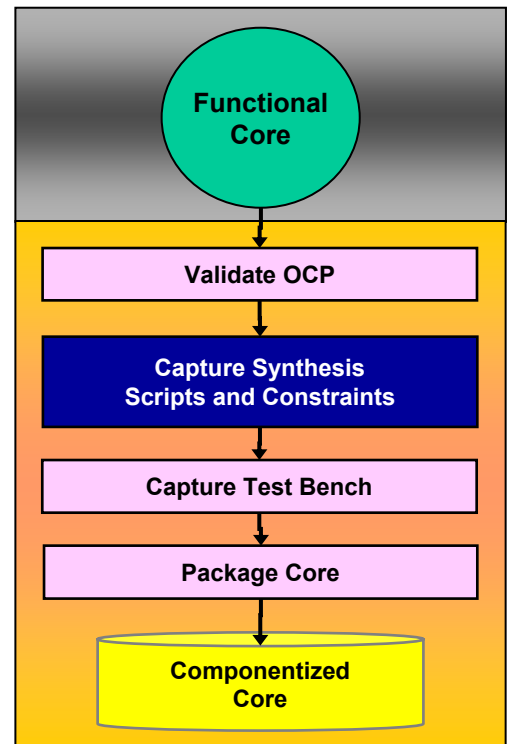
Benefits

Rapid Time to Market

- Streamlines and automates OCP validation
- Decouples core and system development
- Enables multiple cores to be developed in parallel
- Provides a structured core debug and verification environment allowing system-level design verification

Complete IP Reuse

- Standardizes core I/O
- Builds portable test bench



Streamlined OCP validation and componentization

The complete Open Core Protocol Specification is available at www.ocpip.org

CoreCreator

EDA Tools Supported

Simulation

NC Verilog™, Verilog-XL™ by Cadence Design Systems
VCS by Synopsys, Inc.
ModelSim™ by Model Technology

Synthesis

Design Compiler™ by Synopsys, Inc.

Static Timing Analysis

PrimeTime™ by Synopsys, Inc.

Platforms Supported

Sun Solaris 5.8 and 5.9
RedHat Linux 7.2, 7.3 and Enterprise Workstation 3.0

Related Documents

- Open Core Protocol Reference

EDA Tools Included

Tools

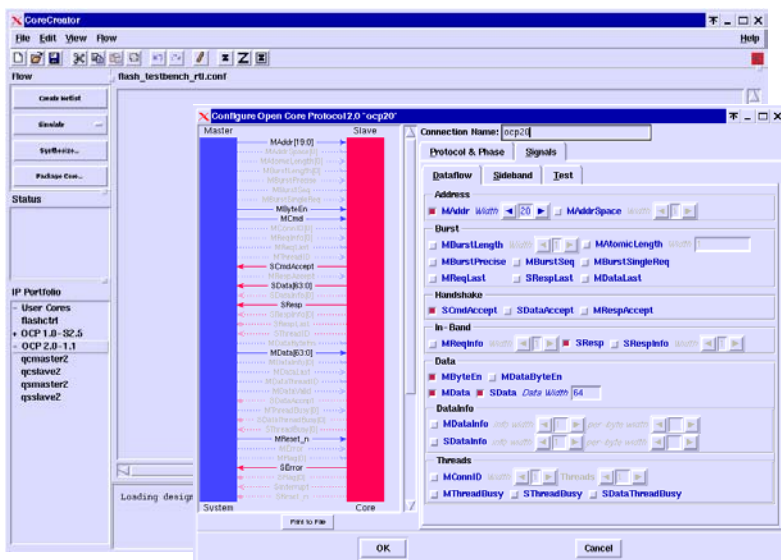
coreclean
corecomp
corecreator
coremap
corepackage
ocpcheck2
ocpdis2
ocpperf2
small/simrun
simanalyze
simprepare
socgenerate
techcomp

Removes all corecomp-generated files
Core test bench RTL generator
Graphical user interface
Generates synthesis constraints file
Package core representations for reuse
OCP protocol checker
OCP disassembler
Performance statistics on a given OCP
Simulation commands
Post-simulation analysis
Pre-simulation test preparation
Controls options for RTL generation
Extracts technology parameters from synthesis library

Methods (scripts)

coresimulate
coresynthesize
wglgenerate

Compiles design and initiates simulation
Runs synthesis
Generates WGL file from OCP monitor



The complete Open Core Protocol Specification is available at www.ocpip.org

Ease-of-use with convenient GUI

About OCP-IP®

OCP International Partnership Association, Inc. (OCP-IP) is an independent, non-profit semiconductor industry consortium formed to administer the support, promotion and enhancement of the Open Core Protocol (OCP). OCP is the first fully supported, openly licensed, comprehensive interface socket for semiconductor intellectual property (IP) cores. The mission of OCP-IP is to address problems relating to design, verification and testing which are common to IP core reuse in System-on-Chip (SoC) products. OCP-IP is funded through the annual membership dues of its members: intellectual property, companies, integrated device manufacturers, system companies, EDA providers and design houses. VSIA endorses the OCP socket, and OCP-IP is an Affiliate of the VSI Alliance.

OCP-IP Association, Inc. 3855 SW 153rd Drive, Beaverton, Oregon 97006 USA
Tel: 1-503-619-0505 Fax: 1-503-644-6708 E-mail: admin@ocpip.org URL: www.ocpip.org