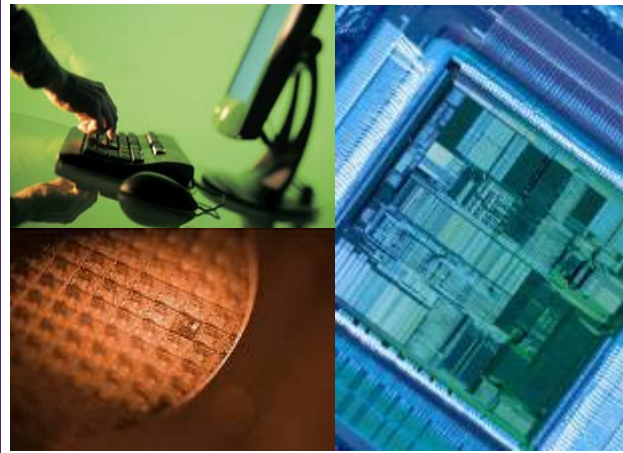













DesignWare Library New OCP Verification IP



SYNOPSYS[®]
Predictable Success

DesignWare® Verification IP (VIP) Portfolio

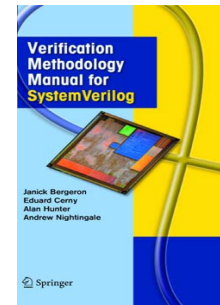
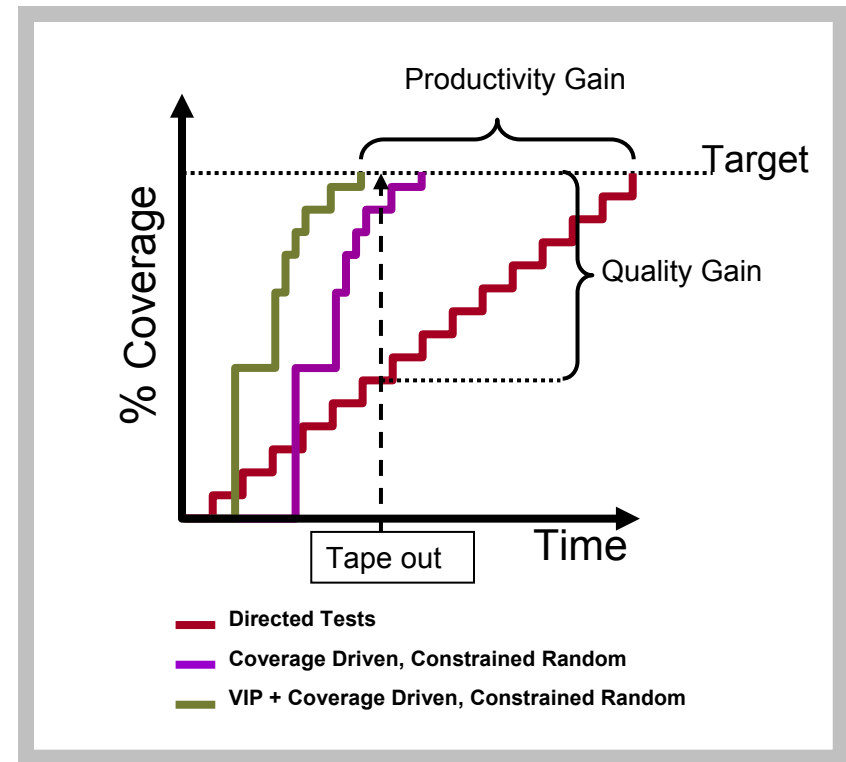
Title		Current Interfaces
AMBA 3 AXI		AXI APB3
AMBA 2.0 AHB, APB		AHB 2.0 APB 2.0
OCP 2.1		OCP 2.1
USB		USB 1.1 USB 2.0 USB OTG
PCI Express		PCIe 1.1 PCIe 2.0
Serial ATA 2.5 Host		Gen I 1.5 Gbps Gen II 3.0 Gbps
10/100/1G/10G Ethernet		XGMII
		XAUI
		SGMII
		RGMII
		GMII
		SMII
		MII
PCI		PCI 2.3
		PCI-X 1.0
		PCI-X 2.0
Serial IO		RS232
		GPIO
		IrDa
I2C		I2C
10,000 Memory Models		SRAM SDRAM, DDR II SDRAM, FLASH, etc



- **Common infrastructure / usage style**
 - Simplifies multiple-model usage
 - Easy to learn new titles
- **Used in a wide variety of environments**
 - Easy to integrate into your current methodology
 - Verilog, SystemVerilog and VHDL
 - All popular simulators
 - Directed and Constrained Random Environments
 - Integrated in Synopsys Discovery™ platform
 - Native for higher performance
 - Verification Methodology Manual (VMM)
- **Used at over 600 customer sites**
 - Proven by 1000s of users

How DesignWare VIP Improves Productivity

- Command-Based Usage
 - Verilog, SystemVerilog or VHDL
 - Read, Write, Burst, etc.
 - Hand-authored tests
 - Tests predicted behavior
- Object-Based Usage
 - Constrained Random Verification
 - Verification Methodology Manual
 - Accelerates time to reach coverage goals
 - Automated tests
 - Functional Coverage Statistics
 - Tests predicted and unpredicted behavior

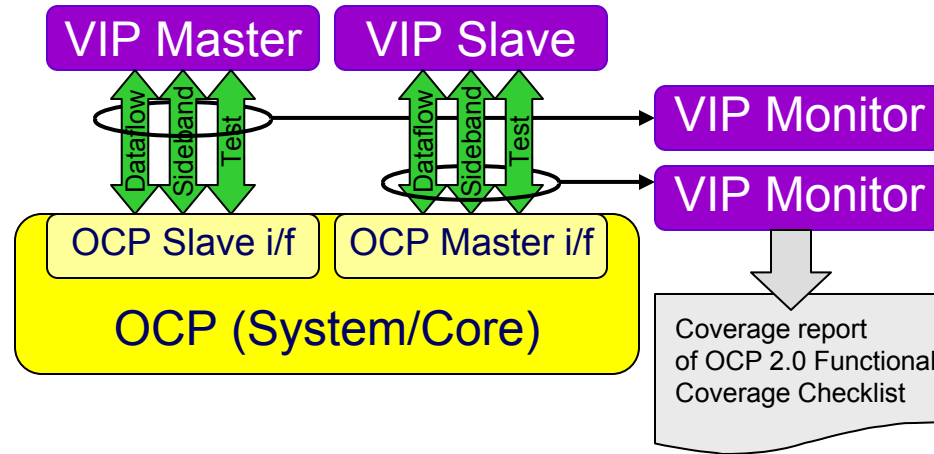


Now Available for OCP Verification

Master, Slave and Monitor Components

- Supports all OCP 2.0/2.1 transaction types
- Master initiates OCP transactions
- Slave responds to transactions initiated by a master
 - Observes the master-driven signals on the bus, and detects the request phase(s) of a transaction to initiate a response procedure
- Monitor observes and reports on OCP bus activity
 - Built-In Functional Coverage of OCP-IP defined functional coverage groups
- Error injection

Supports All OCP 2.1 Configurations

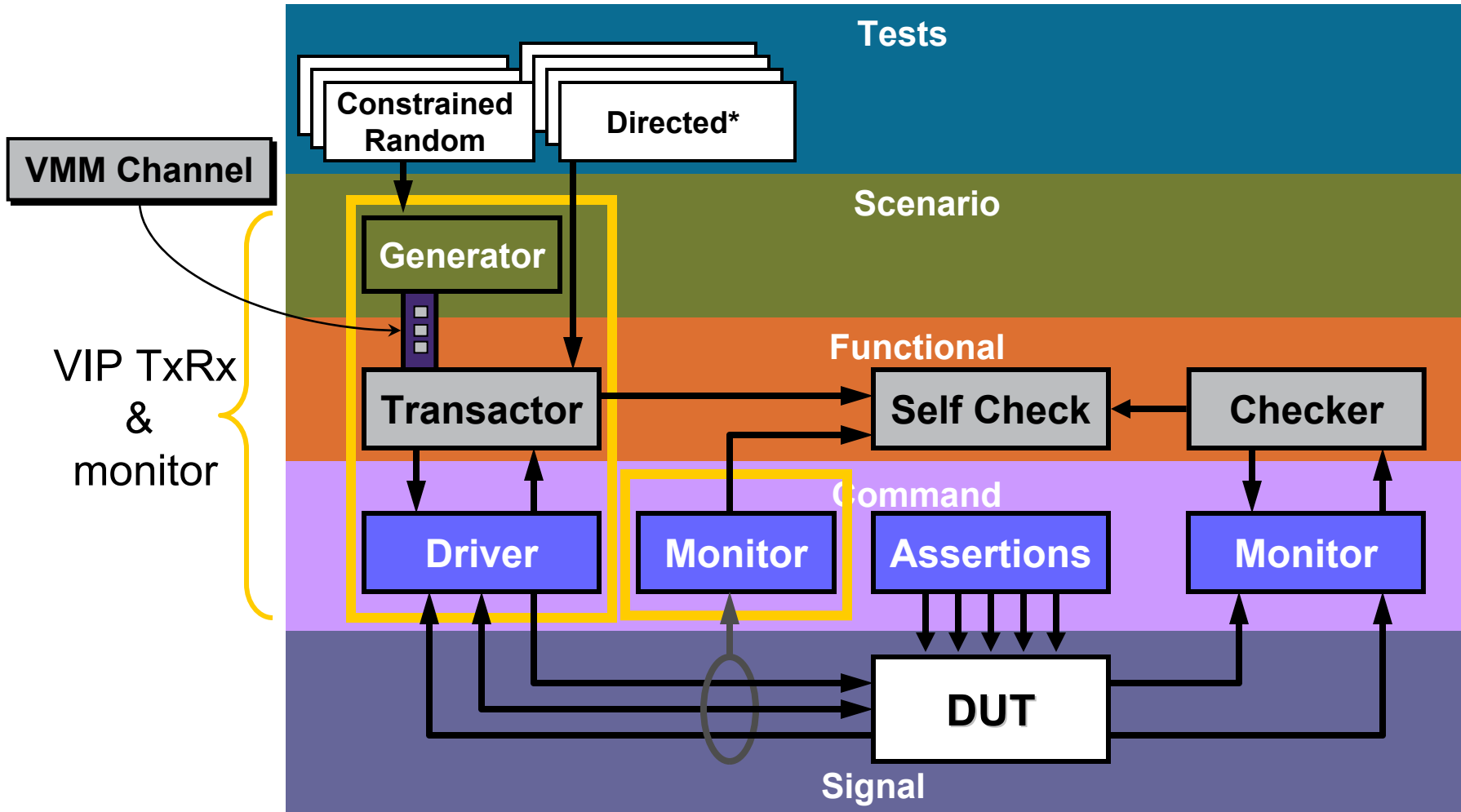


Verification IP configured using configuration data object or HDL commands

- Determines which signals are in interface, how wide they are, number of concurrent transfers, timeouts, burst length, burst type etc.
- Separate configuration for each master, or slave that is on the bus
 - Can be different as long as signals are tied off correctly

Verification IP with VMM

Verification Methodology Manual for SystemVerilog

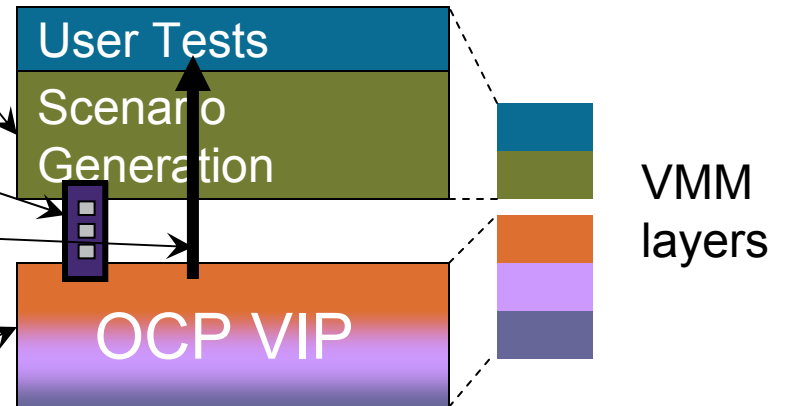


*Users can also create directed tests using VIP

VMM Testbench Usage

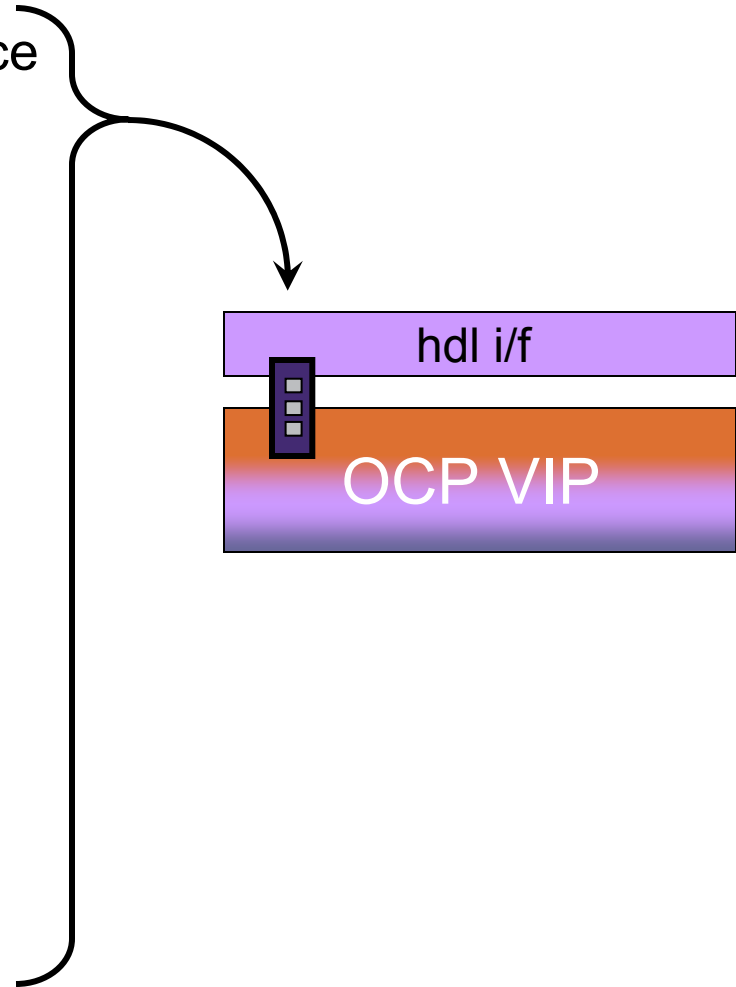
- SystemVerilog Object-based Interface

- Example Scenario Generation
- Channels
 - Input, Output, Activity
- Callbacks
 - Matched with Channels (get, put)
- Transactors
 - Master, Slave, Monitor



HDL Testbench Usage

- SystemVerilog, Verilog, VHDL interface
 - Transactions commands
 - Create New Transactions
 - Apply to Transactor
 - Wait for callbacks, etc.
 - Configuration
 - Create and apply configuration
 - Interrogate configuration, etc.
 - Logging
 - Enable/Disable logging types
 - Change Verbosity
 - Coverage
 - Toggle, Signal, Transaction



How we test DesignWare OCP VIP

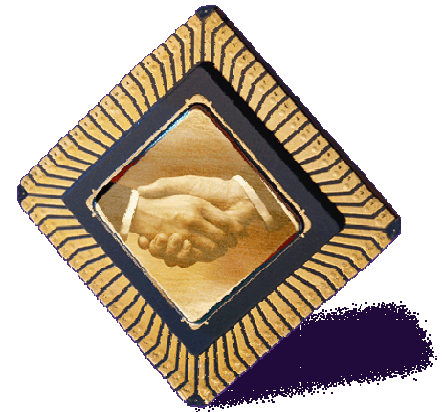
Internal Regression Environment

- Constrained Random Verification
 - Randomized traffic
 - Randomized configurations
 - Some directed tests
- Covers 100% of mandatory coverage points
 - As described in section 4 of the compliance checks document
 - Also includes optional coverage points
- Regression Environment is used as a basis for the testbench example shipped with the Verification IP
 - Includes scenario generators to aid testbench development
 - Includes examples of the tests



DesignWare Verification IP Benefits

- **Saves testbench development time**
 - Easy to integrate into your current methodology
 - Provides coverage reports and protocol checks
- **Reduces project risk**
 - Enables verification of full breadth of each protocol
 - Support for constrained random verification
 - Tests for corner cases behavior
- **Highest quality**
 - Design proven on hundreds of customer designs
 - Extensive regression environments
- **Part of the industry leading verification IP portfolio**
 - Most popular standard bus protocols
 - Broadest collection of verification IP titles



Thank You

- Questions?