SYNOPSYS®
Predictable Success

Is your glass half-empty..
..or half-full?

Using DW VIP for OCP to model best-case, worst case scenarios

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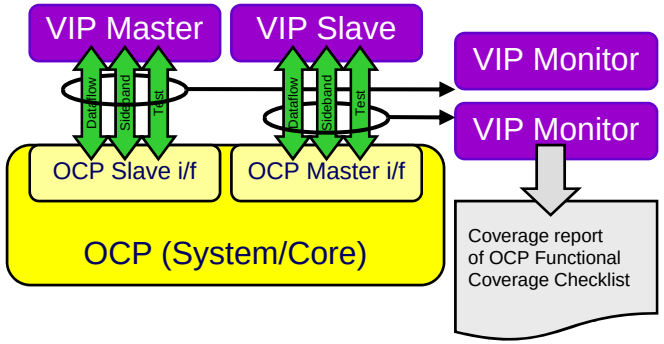
DesignWare Verification IP

DesignWare OCP Verification IP

Supports all OCP 2.0/2.1/2.2 dataflow & sideband transaction types

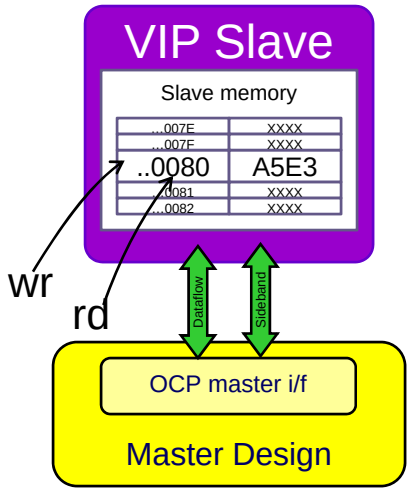


- Master initiates OCP transactions
- Slave observes the master-driven signals on the bus and initiates response procedure
- Monitor observes and reports on OCP bus activity
  - Built-In Functional Coverage of OCP-IP defined functional coverage groups
- Configuration determines which signals are in interface, how wide they are, number of concurrent transfers, timeouts, burst length, burst type etc

Slave Memory Access

Not always so straightforward

- Reading/Writing to the same address in a slave design may result in Hazards
  - Success depends on Slave Memory characteristics
- Need to model this in verification
  - When is data committed to memory?
  - When should the master begin a request phase?
  - When should the master begin datahandshake?



So are you an optimist?

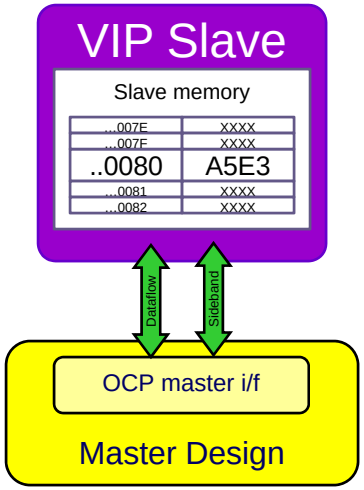
- When is data committed to slave memory?
  - When it is sampled by the slave ….
    …Or when it is accepted by the slave
- When should the request phase of a write transfer begin if there is a previous read with overlapping address?
  - When the response phase from the previous read is started..
    …Or when the response phase is accepted
- When can the datahandshake phase of a transfer start?
  - When the request is started….
    …Or when the request is already accepted
  - And if there is a previous READ with an overlapping address; when the response phase is started…
    …Or when the response phase is already accepted

The Good News!

You can control it all with DW OCP VIP

- DW VIP gives you more control
  - New: Control potential hazards from reads and writes to the same address
    - A read following a write may cause a hazard if the slave has not committed the write data to memory
    - A write following a read may cause a hazard if the Slave commits the data to memory too soon (prior read response may return new write data).
  - Control Backpressure from consecutive transactions to the same slave
    - Semi-randomize delayed response from the slave

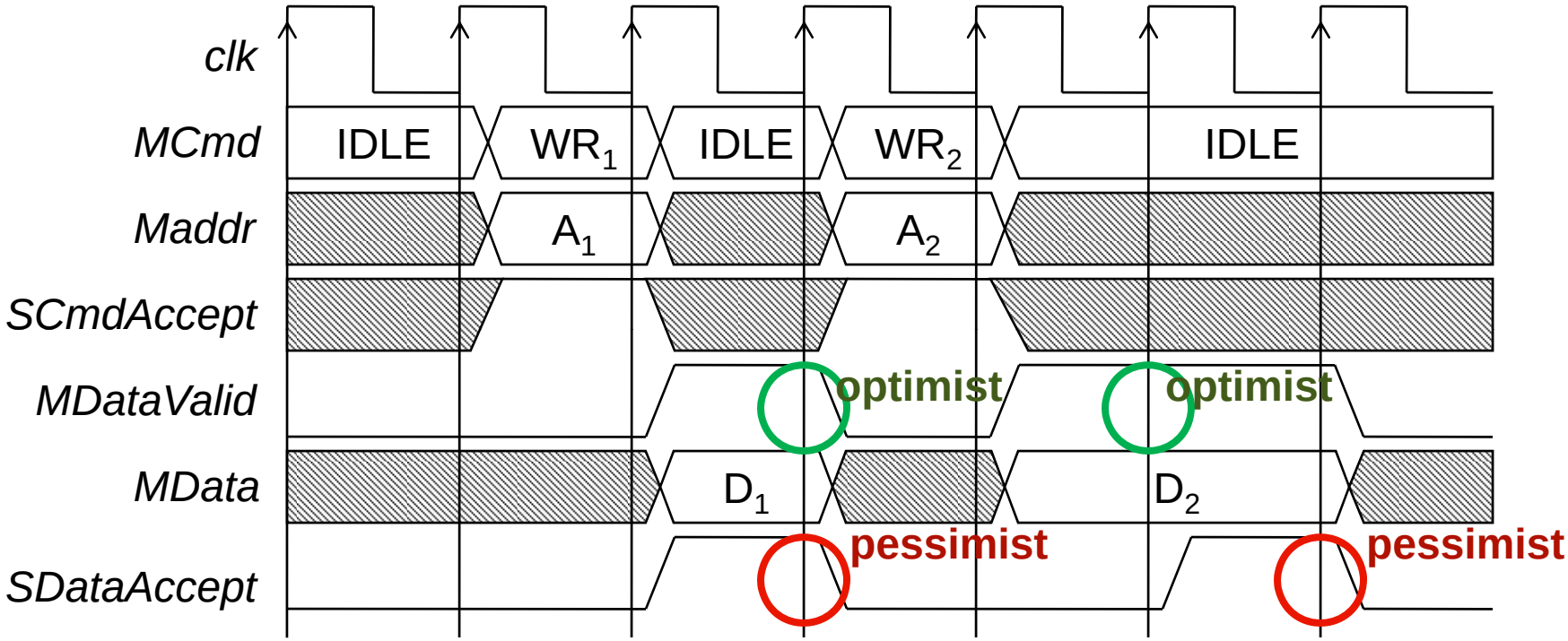
DW Verification IP (Slave)
Testing a master interface



- User controls when Data is committed to memory
  - Optimistic
    - With datahandshake: when MDataValid is high
    - Without datahandshake: when request is sampled
  - Pessimistic
    - With SDataAccept: when SDataAccept is high
    - Without SDataAccept: when data is sampled
- Backpressure options for slave VIP
    - FIFO on outstanding requests,
    - Buffer on requests vs repsonses
    - Outstanding datahandshake vs response

* or if reqdata_together is used

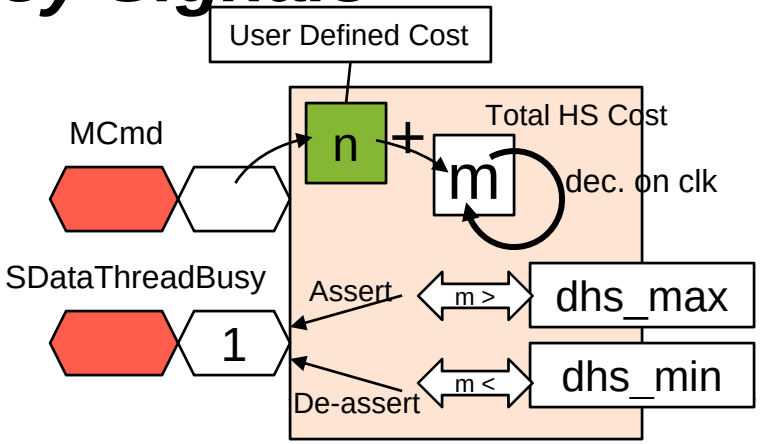
When is data committed to the slave VIP memory?



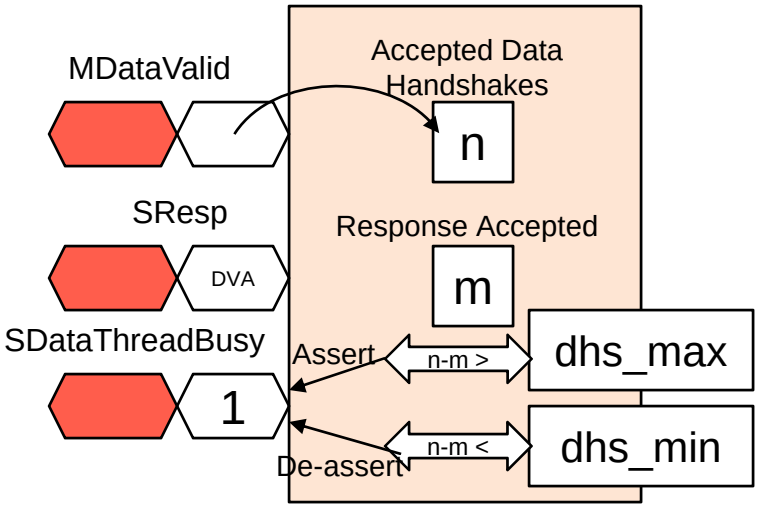
- With datahandshake in the interface
  - Optimitist: When MDataValid goes high
  - Pessimist: When SDataAccept goes high

Backpressure Options for Slave
Automated SDataThreadBusy Signals

- FIFO Method
  - Each new request adds a user defined handshake cost to the total cost for the thread
  - VIP compares total cost to user defined dhs_max and dhs_min values
    - Asserts SDataThreadBusy
  - Decrements cost by one on each clock

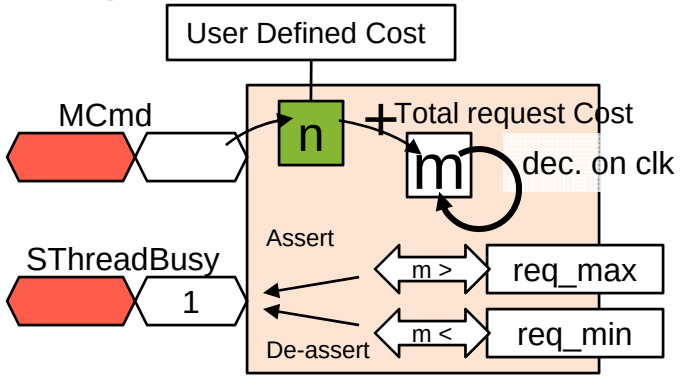


- Response Method
  - VIP monitors accepted response pipeline and data handshake pipeline
    - Depends on write transactions that require responses
  - Calculates the difference between datahandshake queue and response queue, and compares to dhs_max and dhs_min set by user
    - Asserts SDataThreadBusy

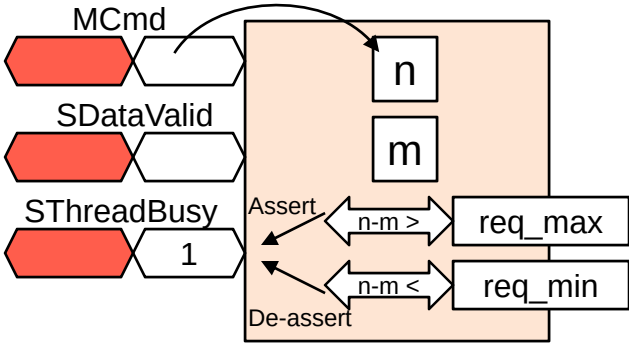


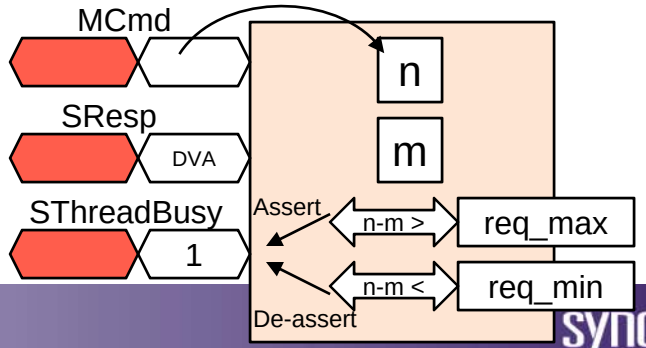
Backpressure Options for Slave
Automated SThreadBusy Signals

- FIFO method
  - Each new request adds a user defined request cost to the total cost for the thread
  - VIP compares total req cost to user defined req_max and req_min values
    - Asserts SThreadBusy
  - Decrements cost by one on each clock

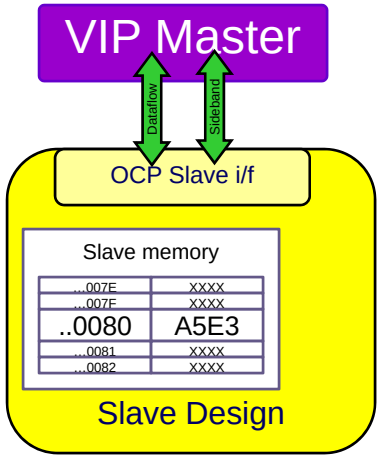


- Outstanding DataHandshake / Response Methods
  - Data (Write Transactions Only, using Data Handshake Pipeline)
    - VIP monitors difference between the number of accepted requests (n) and completed handshakes(m) , and compares to req_max / req_min values
  - Response (using response Pipeline)
    - VIP monitors the difference between the number of accepted requests (n) and number of responses accepted (m) and compares to
    - req_max and req_min values
  - Asserts SThreadBusy





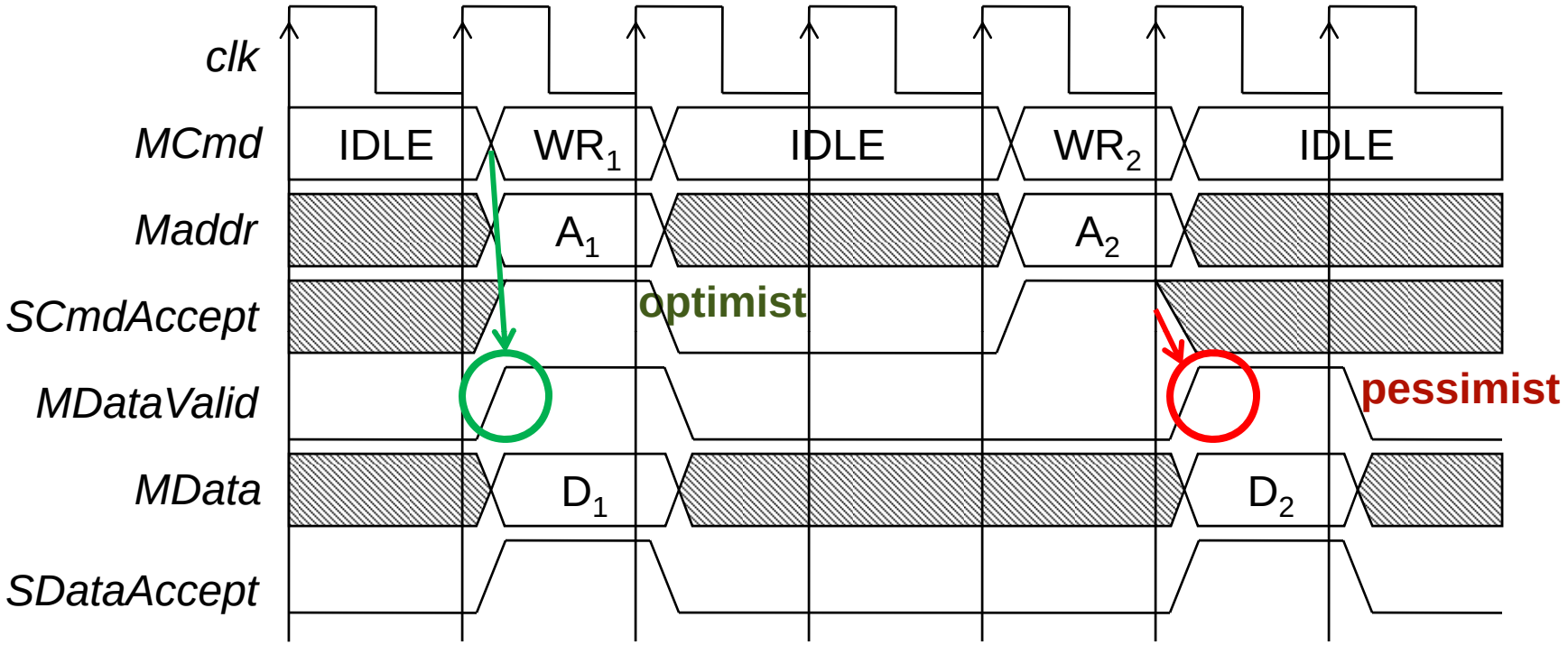
DW Verification IP (Master) Testing a slave interface



- Set when datahandshake may start
  - Request has started OR has been accepted
  - When a previous READ with overlapping address…
    - Response phase has started OR has been accepted
- Sets when request phase may start when datahandshake not used in interface* (Master)
  - When a previous READ with overlapping address…
    - Response phase has started OR has been accepted
- Backpressure options for Master
  - FIFO on responses

* or if reqdata_together is used

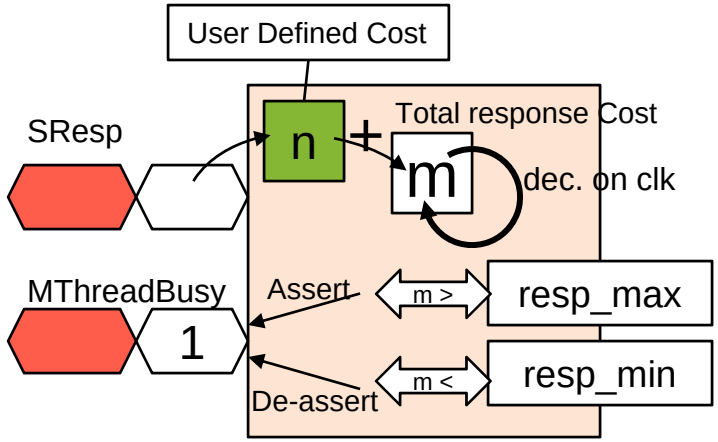
When can a Master begin datahandshake?



- With datahandshake in the interface
  - Optimitist: datahandshake begins when request started
  - Pessimist: datahandshake begins when request accepted

BackPressure for Master VIP
Automated MThreadBusy Signals

- Each new queued response adds a user defined response cost to the total cost for the thread
- VIP compares total response cost to user defined value
  req_max and req_min values
  - Asserts MThreadBusy
- Decrements cost by one on each clock

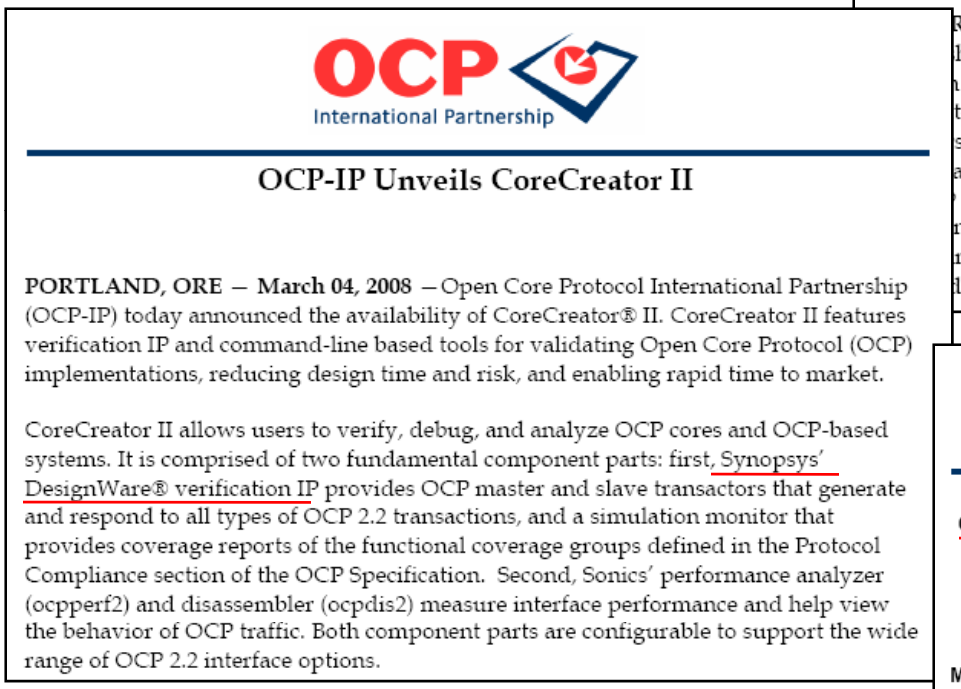


DesignWare Verification IP for OCP

Lets you control Slave memory access

- Timing of Handshaking and Requests initiated by master
- Control of when data is committed to slave memory
- Simulated backpressure in master and slave VIP

DesignWare VIP for OCP

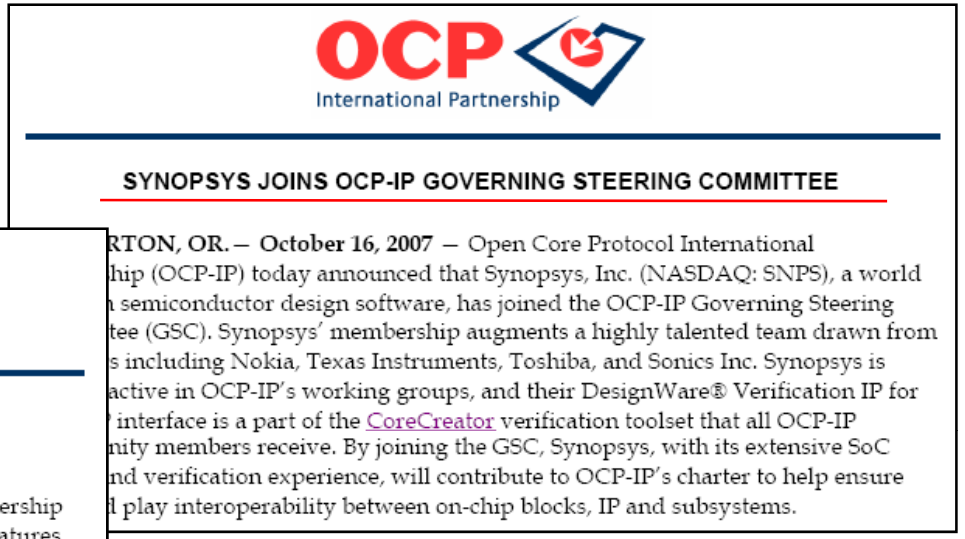


OCP International Partnership

OCP-IP Unveils CoreCreator II

PORTLAND, ORE — March 04, 2008 —Open Core Protocol International Partnership (OCP-IP) today announced the availability of CoreCreator® II. CoreCreator II features verification IP and command-line based tools for validating Open Core Protocol (OCP) implementations, reducing design time and risk, and enabling rapid time to market.

CoreCreator II allows users to verify, debug, and analyze OCP cores and OCP-based systems. It is comprised of two fundamental component parts: first, Synopsys' DesignWare® verification IP provides OCP master and slave transactors that generate and respond to all types of OCP 2.2 transactions, and a simulation monitor that provides coverage reports of the functional coverage groups defined in the Protocol Compliance section of the OCP Specification. Second, Sonics' performance analyzer (ocpperf2) and disassembler (ocpdis2) measure interface performance and help view the behavior of OCP traffic. Both component parts are configurable to support the wide range of OCP 2.2 interface options.



OCP International Partnership

SYNOPSYS JOINS OCP-IP GOVERNING STEERING COMMITTEE

RTON, OR. — **October 16, 2007** — Open Core Protocol International
hip (OCP-IP) today announced that Synopsys, Inc. (NASDAQ: SNPS), a world
semiconductor design software, has joined the OCP-IP Governing Steering
tee (GSC). Synopsys' membership augments a highly talented team drawn from
s including Nokia, Texas Instruments, Toshiba, and Sonics Inc. Synopsys is
active in OCP-IP's working groups, and their DesignWare® Verification IP for
interface is a part of the CoreCreator verification toolset that all OCP-IP
nity members receive. By joining the GSC, Synopsys, with its extensive SoC
nd verification experience, will contribute to OCP-IP's charter to help ensure
l play interoperability between on-chip blocks, IP and subsystems.

OCP International Partnership

OCP-IP STANDARDIZES ON SYNOPSYS' DESIGNWARE VERIFICATION IP FOR OCP-IP'S CORECREATOR VERIFICATION TOOLSET

Collaboration Delivers OCP-compliant Verification Solution for Improved Interoperability and Quality of OCP designs

MOUNTAIN VIEW, Calif. and BEAVERTON, OR – April 10, 2007 - Synopsys, Inc. (Nasdaq:SNPS), a world leader in semiconductor design software, and Open Core Protocol International Partnership (OCP-IP), an independent non-profit semiconductor industry consortium, today announced that they are collaborating to provide Synopsys' DesignWare® Verification IP (VIP) as part of OCP-IP's CoreCreator verification toolset. DesignWare VIP for OCP, part of Synopsys' portfolio of standards-based verification IP, will become the OCP-IP endorsed verification IP solution and will replace the OCP Bus Functional Models (BFM) currently provided with OCP's CoreCreator tool. The new, combined solution, which includes DesignWare VIP and CoreCreator's performance analysis, protocol checking, and transaction disassembly, gives OCP-IP members a common verification toolset, enabling maximum consistency and interoperability across OCP implementations. The collaboration also further expands OCP-IP's robust thriving infrastructure.

DesignWare® Verification IP (VIP) Portfolio

Title	Current Interfaces
AMBA 3 AXI	AXI
	APB3
AMBA 2.0 AHB, APB	AHB 2.0
	APB 2.0
OCP 2.2	OCP 2.0/2.1/2.2
USB	USB 1.1
	USB 2.0
	USB OTG
PCI Express	PCIe 1.1
	PCIe 2.0
Serial ATA 2.6 Device	Gen I 1.5 Gb/sec
	Gen II 3.0 Gb/sec
	6.0 Gb/sec
10/100/1G/10G Ethernet	XGMII, XAUI
	GMII, RGMII, SGMII
	MII, RMII, SMII
	TBI
PCI	PCI 2.3
	PCI-X 1.0, 2.0
Serial IO	RS232
	GPIO
	IrDa
I2C	I2C

- **Common infrastructure / usage style**
  - Simplifies multiple-model usage
  - Easy to learn new titles
- **Used in a wide variety of environments**
  - Easy to integrate into your current methodology
    - Verilog, SystemVerilog and VHDL
    - All popular simulators
    - Directed and Constrained Random Environments
  - Integrated in Synopsys Discovery™ platform
    - Native for higher performance
    - Verification Methodology Manual (VMM)
- **Used at over 600 customer sites**
  - Proven by 1000s of users

DesignWare Verification IP Benefits

- **Saves testbench development time**
  - Proven standard testbench components that you don't need to write and support
  - Easy to integrate into your current methodology
- **Reduces project risk**
  - Enables verification of full breadth of each protocol
  - Support for constrained random verification
    - Tests for corner cases behavior
  - Provides coverage reports and protocol checks
- **High quality**
  - Design proven on hundreds of customer designs
  - Extensive regression environments