

MIPS TECHNOLOGIES INTRODUCES NEW MICROARCHITECTURE FOR THE NEXT-GENERATION OF EMBEDDED DESIGNS

*MIPS32™ 24K™ Microarchitecture Basis for Family of Highest-Performance, Synthesizable Cores Available
for Licensing*

SAN JOSE, CAL. Embedded Processor Forum - June 16, 2003 - MIPS Technologies, Inc. (Nasdaq: MIPS, MIPSB), today introduced a new high-performance microarchitecture that will address the changing economics of SOC design and help engineers increase profitability by extending their product's lifecycle. The MIPS32™ 24K™ microarchitecture is the foundation for MIPS Technologies' next-generation of high-performance, synthesizable cores, and extends the company's leadership as the provider of industry-standard performance technology to semiconductor and system companies.

The economics of SOC design are rapidly changing as process technologies migrate to 0.13µm and below causing fixed design costs, such as mask sets, to explode. As a result, system companies are under increasing pressure to maximize profitability by extending their products' time in market without new silicon spins. Using high performance, programmable technology, such as the MIPS32 24K microarchitecture, SOC designers can leverage falling transistor costs to implement hardwired functionality in software.

"The high performance and programmable capabilities offered by the 24K microarchitecture enable system designers to add the features that their customers demand in software instead of using expensive mask sets," said Mike Uhler, CTO for MIPS Technologies. "Combined with the more than 20 years of software development around the industry-standard MIPS architecture, customers can leverage the investment in operating systems, optimized protocol stacks and tool chains to reduce overall product development costs while getting to market faster."

Applications

The MIPS32 24K microarchitecture is well suited for next-generation embedded devices, such as digital consumer devices like set-top boxes and digital televisions, where high levels of system performance and application configurability are required. Furthermore, the 24K microarchitecture meets the emerging service demands in broadband access and evolving networking infrastructure protocols that require software programmability.

The new microarchitecture from MIPS Technologies was designed based upon feedback from market-leading customers who are looking to offer new feature rich products to the digital consumer and networking market segments. It is designed to scale beyond 0.13µm process technologies and features the latest architectural enhancements and configurable features from MIPS Technologies while maintaining compatibility with the industry-standard MIPS32 architecture.

"The 24K microarchitecture was designed in response to our customers' need for synthesizable and high-performance solutions," said Jack Browne, vice president of worldwide sales. "The name of the game is getting a differentiated product to market ahead of the competition-and the 24K microarchitecture enables our customers to do just that."

Features of the MIPS32 24K Microarchitecture

The new MIPS32 24K microarchitecture is ideal for products requiring high frequency operation on a low power budget. As with all MIPS-based™ technologies, it offers broad tool and software support only available to products based upon an industry-standard architecture. It delivers the highest performance in its class with unique features such as:

Scalable performance:

- Single issue, 8-stage pipeline
- Operating performance ranges from 400 to 550 MHz (worst case) in a 0.13 processes

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- Architected for scalability beyond 0.13µm technology nodes
- Hardware-based cache coherency to support multi-processor scaling
- Configurable memory management unit with TLB or fixed mapping
- 64-bit high performance memory subsystem with up to six outstanding read transactions

Implementation of the MIPS32 architecture:

- Release 2 implementation with features such as multiple general purpose register sets and support for vectored interrupts
- Reduced interrupt latency
- Code compression technology with MIPS16e™ ASE

Fits industry-standard SOC construction methodologies:

- Fully synthesizable
- OCP high-speed point-to-point on-chip interconnect

Optimized for market-specific implementations:

- User extendable instructions with the CorExtend™ feature
- Floating point support that is fully compliant with IEEE 754
- Advanced power management features

Fits low-cost requirements for embedded designs:

- Application configurability to optimize area and features
- Compact core - optimal die size
- Code size efficiency

Design time reduction:

- Maintains compatibility with the industry-standard MIPS32 architecture
- Enables access to the broad array of third party tools and software
- Leverages the extensive software investments in the MIPS32 architecture, such as middleware and application software, made by MIPS® partners during the past twenty years

Forward Concepts

"MIPS Technologies has recognized that the economics of silicon are changing, and extending a product's time in market is critical to profitability," said Will Straus, founder and president of Forward Concepts. "The 24k microarchitecture is a direct response to these trends, bringing high performance and programmability to solve the business challenges of next-generation SOC design."

Green Hills Software

"The 24K microarchitecture is a welcome addition to the SOC market. We're pleased to be part of this exciting new offering," said Christopher Smith, vice president of marketing for Green Hills Software. Green Hills Software will provide development tools and operating system support for the 24K microarchitecture. "Green Hills products and cores based upon the 24K microarchitecture provide a winning combination and will significantly benefit customers facing the challenges of next-generation SOC design," continued Uhler from MIPS Technologies.

Jim Turley

"The 24k microarchitecture extends MIPS Technologies' position as the unquestioned high-performance leader within the embedded market. The combination of high scalar performance and embedded sophisticated coherency will further establish MIPS Technologies as the solution for anyone developing high-performance, multi core SOC's," said Jim Turley, founder and editor of the Silicon Insider.

OCP International Partnership

"I am pleased to see the continuing momentum of OCP reflected in MIPS Technologies' strategic adoption of OCP in their new microarchitecture," said Ian Mackintosh, president of OCP-IP. "The wide range of IP available and the tools infrastructure provided by OCP-IP make it a natural choice for high-end embedded designs."

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WindRiver Systems

"WindRiver and MIPS Technologies have a long history of developing optimized platform solutions for the digital consumer and networking markets," said Larry MacFarlane, general manager of the network infrastructure group for Wind River Systems. "The high-performance 24K microarchitecture is ideally suited to address the needs of our customers within these target markets. Together, 24K and our WindRiver Platforms will further speed the time-to-market parameters of our customers, while reducing risk and overall product cost."

Availability

Core derivatives based upon the MIPS32 24K microarchitecture will be available to early access customers by the fourth calendar quarter of 2003, and available for general licensing in the first calendar quarter of 2004.

About MIPS Technologies

MIPS Technologies, Inc. is a leading provider of industry-standard processor architectures and cores for digital consumer and business applications. The company drives the broadest architectural alliance that is delivering 32- and 64-bit embedded RISC solutions. The company licenses its intellectual property to semiconductor companies, ASIC developers and system OEMs. MIPS Technologies and its licensees offer the widest range of robust, scalable processors in standard, custom, semi-custom and application-specific products. The company is based in Mountain View, Calif., and can be reached at +1 (650) 567-5000 or www.mips.com

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