OCP International Partnership

THE COMPLETE SOCKET

OCP-IP: Supporting ESL

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Agenda

- OCP-IP introduction
- OCP-IP vision
- Importance of infrastructure
- OCP-IP infrastructure and Working Groups
- Example of work in SystemC arena
- Real world value: Texas Instruments OMAP platform

OCP-IP Mission

"….to promote and support OCP as the complete socket standard that ensures rapid creation and integration of interoperable virtual components."

Membership: Board, Sponsors, Universities, etc.

- 3Plus1 Technology
- AccelChip
- Accent
- Acculent Corporation
- Actvision
- Advanced Architectures
- Alcatel
- Alpha Data
- Amphion Semiconductor
- ARC International
- Artec Design Group
- Arteris
- Artisan Components
- ASICS World Services
- ATI Technologies
- Atrenta
- Beach Solutions
- Bitboys
- BlueSpec
- Broadcom
- Cadence Design Systems
- Carbon Design Systems
- CAST, Inc.
- CCLRC
- Celoxica
- Chip Implementation Center
- Cologne Chip
- ControlNet India
- CoWare
- CSIP
- DAFCA
- Denali
- Design And Reuse
- Digital Media Professionals
- Dolphin Integration
- Duolog
- Doulos
- eASIC
- Ecole Polytechnique de Montreal
- EDA Consortium
- ECSI
- EDACafe
- eInfochips
- Ernst & Young, LLP
- Esterel Technologies
- European Space Agency
- Evatronix
- First Silicon Solutions
- Flextronics Semiconductor
- Forte Design Systems
- FueTrek
- GDA Technologies
- GeoLogic
- Georgia Tech
- GreenSocs
- Hantro Products Oy
- HDL Design House
- Hughes Network Systems
- IBM
- Icera Semiconductor
- IDT
- Imagination Technologies
- Infineon
- Inicore
- IPTC
- ITRI
- Jasper Design Automation
- Jeda Technologies
- Jetstream
- Kawasaki Microelectronics
- Leiden University
- LIRMM
- LSI Logic
- LTRIM Technologies
- Manhattan Routing, Inc.
- Marvell
- Mentor Graphics
- Mercury Computing Systems
- Micronas
- MIPS Technologies
- MIT
- MITRE Corporation
- Nallatech
- Nascentric
- National Tsing Hua University
- NEC
- NoBug
- Nokia
- nVIDIA
- Open SysetmC Initiative (OSCI)
- OnDemand Microelectronics
- Paradigm Works
- Perfectus
- Philips Semiconductors
- Pixelworks
- Polarity
- ProDesign
- Prosilog
- PUCRS
- Qualcore Logic
- QThink
- Realtek
- Savant Company
- Ricoh
- Royal Institute of Technology
- sci-worx
- Shenzen Graduate School of Harbin Institute of Technology
- Si2
- Siemens
- Silicon & Software Systems
- Silicon Interfaces
- Silicon Designs International
- Silistix LTD.
- SIPAC
- Sonics
- SpiraTech
- SSIPEX
- STARC
- STMicroelectronics
- Summit Design
- Synergetic Computing
- Synfora
- Synopsys
- System Design Frontiers
- Tampere University of Technology
- Technical University of Denmark
- TechOnLine
- Temento
- Tensilica
- Teradici
- Texas Instruments
- Toshiba Semiconductor Group
- Tower Semiconductor
- TransEDA
- TranSwitch
- TrustIC Design SRL
- TSMC
- UFCG
- UMC
- University of Bologne, Italy
- University of British Columbia
- Université de Bretagne Sud
- University of Houston
- UC Berkeley
- VaST
- VDEC
- Virtual Component Exchange
- Virtual Silicon
- VSIA
- VTT Electronics
- White Eagle Systems Technology
- WiQuest Communications
- Xilinx
- Yamaha Corporation
- YogiTech
- Zuken

OCP – Applications Served – 100's Mu's

Settop Box

Printers

Mobile Phones

Wireless LAN

Games

Video Recorder

DTV's

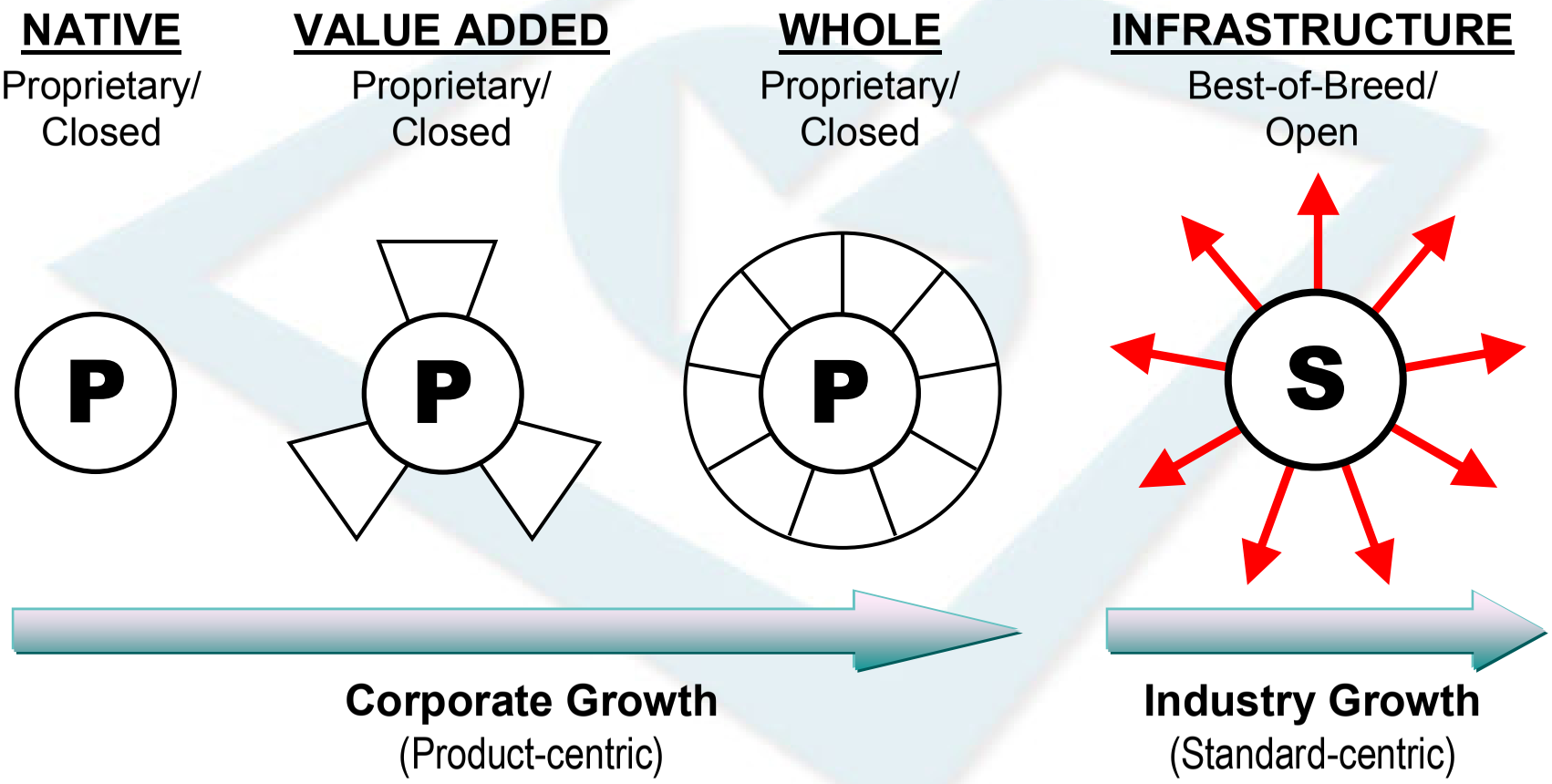
OCP-IP in Asia: Supporting Global Design

- Multiple, existing local-language websites:
  - Japanese, Chinese and Korean
  - Reach homepages via www.ocpip.org
- Technical support in Japanese, available now
  - Contact jptech@ocpip.org
- OCP and CoreCreator Training in Japanese, available now
  - Contact admin@ocpip.org
- Expansion planned into India, CY 2006
  - Several Indian companies already hold OCP-IP membership

Important OCP Facts

- ONLY complete and proven SoC socket
- Essential for “reuse without rework”
  - The only path to Plug and Play
- NOT tied to any one supplier
  - Tools/Interconnect/Design style, Independent
  - Specification freely available
- Full Corporate Presentation available: www.ocpip.org

OCP-IP Industry Vision: Open Standards



Source: Mackintosh Model

Infrastructure for Standards

- What is Infrastructure?
  - The surrounding services, tools, technology, products and information that support the standard

- Importance of Infrastructure:
  - Increases VALUE of Standard
  - SIMPLIFIES adoption: less internal work!
  - Maximizes resource SHARING
  - Lowers COSTS
  - Leverages EXPERT knowledge, etc.

Extensive OCP Infrastructure

View @ www.ocpip.org

OCP-IP Working Groups: Building Infrastructure

- Vision
- Marketing
- Specification
  - Cache Coherence
  - Memory Semantics
- System-Level Design
- Verification
- Debug
- NoC Benchmarking

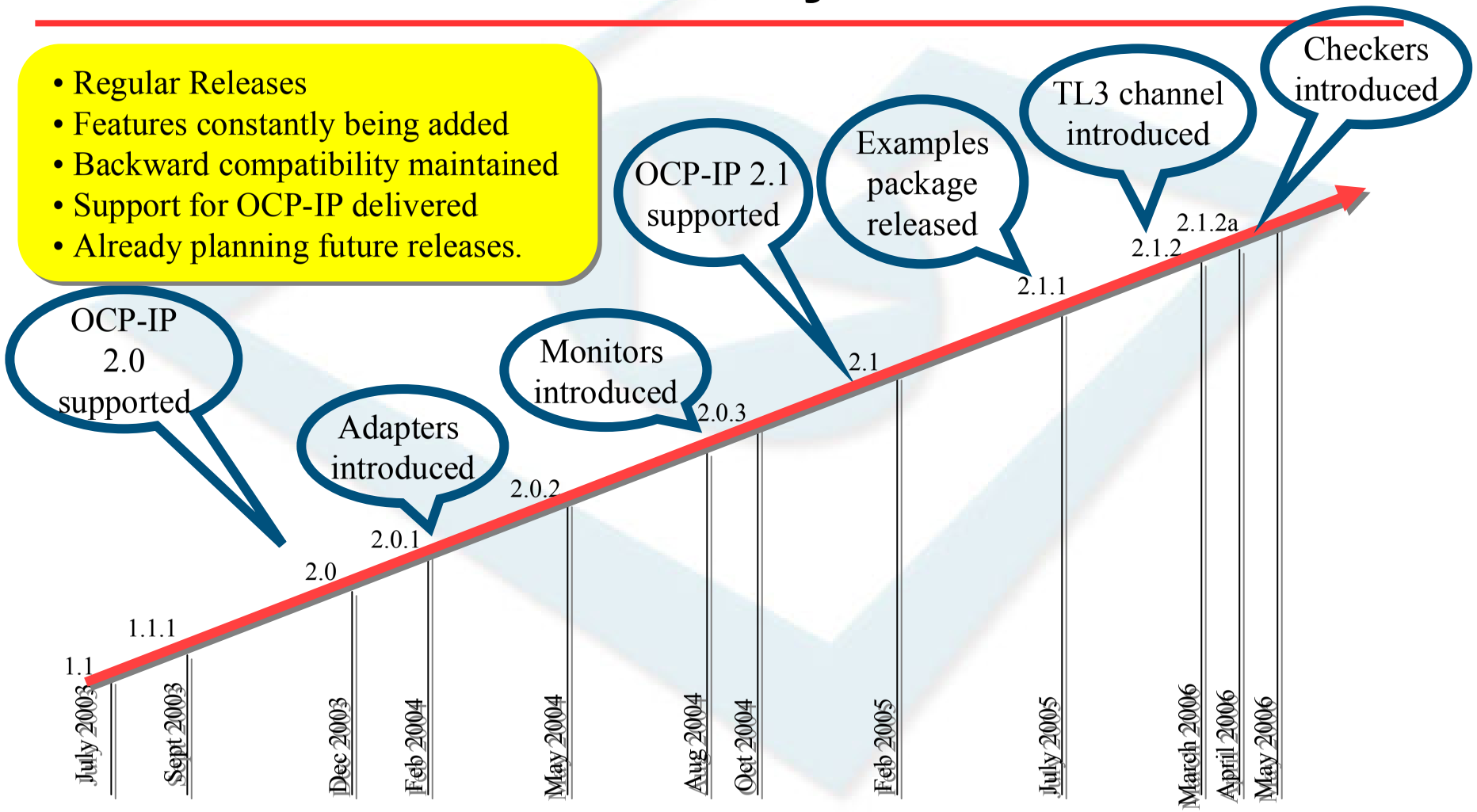
…all groups meet weekly or bi-weekly
Participation: industry leaders/experts

System Level Working Group (SLDWG)

- **ONE** example of value for OCP-IP members
- Extensive record of delivery with SystemC
  - Original work with Transactional Level Models (TLM's)
  - Prolific usage in Industry

OCP-IP's SLDWG: History

- Regular Releases
- Features constantly being added
- Backward compatibility maintained
- Support for OCP-IP delivered
- Already planning future releases.



SLDWG's Package Features

- SLD package (2.1.2a)
- Compatible with OCP-IP 2.1
- All abstraction levels supported : Support for Architects, Designers and Programmers
- Highly configurable channel, with built in sanity checks
- Adapters to go between abstraction levels
- Monitor for performance analysis
- Compatible with OSCI TLM 1.0.
- 130 page documentation of the TLM Communication Channel
- White papers covering OCP's approach to TLM modeling

>14,000 downloads of White paper, >3500 downloads of kit.

All Available to members on line at: www.ocpip.org/members/systemc/

Description: OCP-IP TLM Abstraction Levels

Communication Accuracy		Data Accuracy	Timing Accuracy	Addressed Design Problems
domain specific MoC		tokens	causality, partial event ordering	algorithm design
TLM	TL3	packets	total event ordering, burst-level annotation	functional specification, generic architecture exploration
	TL2	burst of words	burst-level and word-level annotation	exploration of OCP based architecture
	TL1	word	cycle accurate	100% cycle accurate performance profiling
RTL		bitvector	cycle accurate	synthesis

OCP-IP Collaboration with OSCI

- OCP-IP is helping OSCI standardise on the interoperability between models.
- OCP-IP is committed to continuing to ensure that the OCP-IP SLD packages are compatible with the OSCI standard, while continuing to support the wealth of existing OCP-IP based models.
- Members of the OCP-IP SLD WG are key contributors to the OSCI TLM WG.
- OCP-IP has senior technologist formally recognised as a “Key Contributor” to OSCI.
- OCP-IP has already contributed Bus Attribute sets to OSCI, based on OCP-IP’s extensive experience in System Level Design.

CoWare's Valued Contribution at OCP-IP

- CoWare were joint winners of the OCP-IP Outstanding Contributor of the year in 2005 for their contributions to the SLD Working Group.

- CoWare's significant contributions have been:
  - TL3 channel for architectural modeling (CoWare)
    - The TL3 channel enables fast models to be written that can be used by programmers.
    - These sort of models are the key driver for ESL adoption.
  - Unified monitor API (CoWare)
    - Similar API for TL1, TL2, and TL3
    - Enable user-defined OCP monitors
    - Hook arbitrary number of OCP monitors
    - SCV based (aligned with OSCI)

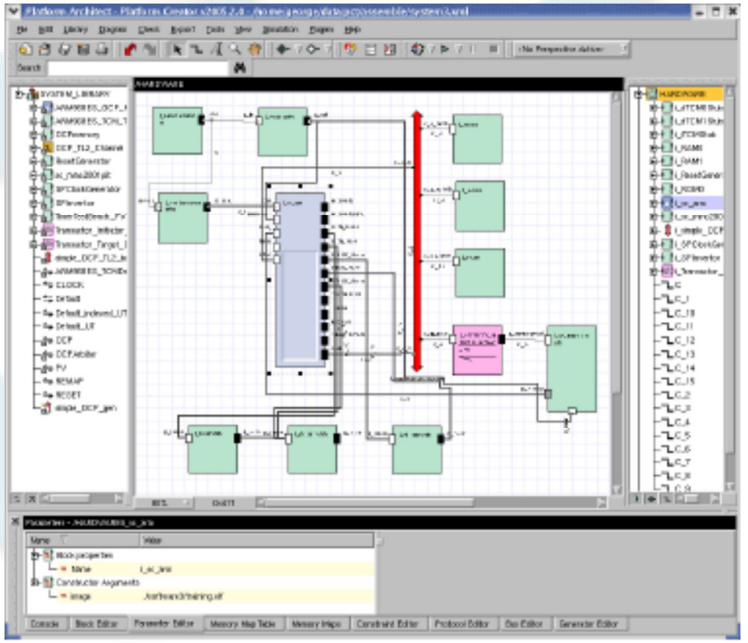
Key Motivator for ESL Adoption:
Start Software Development Early

OCP-IP TL3 models, developed by CoWare are the answer…

TL2 and TL3 Products from CoWare

- Platform Architect, CoWare's flagship product supports both TL2 and TL3 levels of abstraction
- The Architect View Framework's Bus Library contains
  - point-to-point channels,
  - simple shared busses,
  - network-on-chip cross-connect

All supporting protocol agnostic TL3 and OCP-IP TL2 levels of abstraction



OCP-IP Summary

- Organization supports OCP Standard for industry
- Promotes Open Standards and sharing communities
- Provides extensive Infrastructure and Value
- Operates numerous leading-edge Working Groups
- Is extremely active with SystemC
  - TLM original developments
  - Collaboration with industry leaders

- And now, example of OCP-IP Infrastructure in use
  - Texas Instruments OMAP platform…

Modelling OCP-Based SOCs: OMAP-2

James Aldis, TI France

August 2006

OMAP2

- A library of modules for making SoCs for ’phones
  - Processor subsystems, DMAs, interrupt controllers, memory controllers, networks-on-chip, display controllers, security, etc, etc..
  - Consistent design style, timing closure, physical interfaces, programming model
  - *ALL* bus interfaces are OCP-compliant
- A family of TI products based on the library
  - Application processors (OMAP2xxx, 3xxx)
  - Modem processors (OMAPV2xxx, 3xxx)
  - Hybrids
- Platform is OPEN
  - customer is free to do all the software, or take software from TI
- Dominant application processor in 3G mobile ’phone market

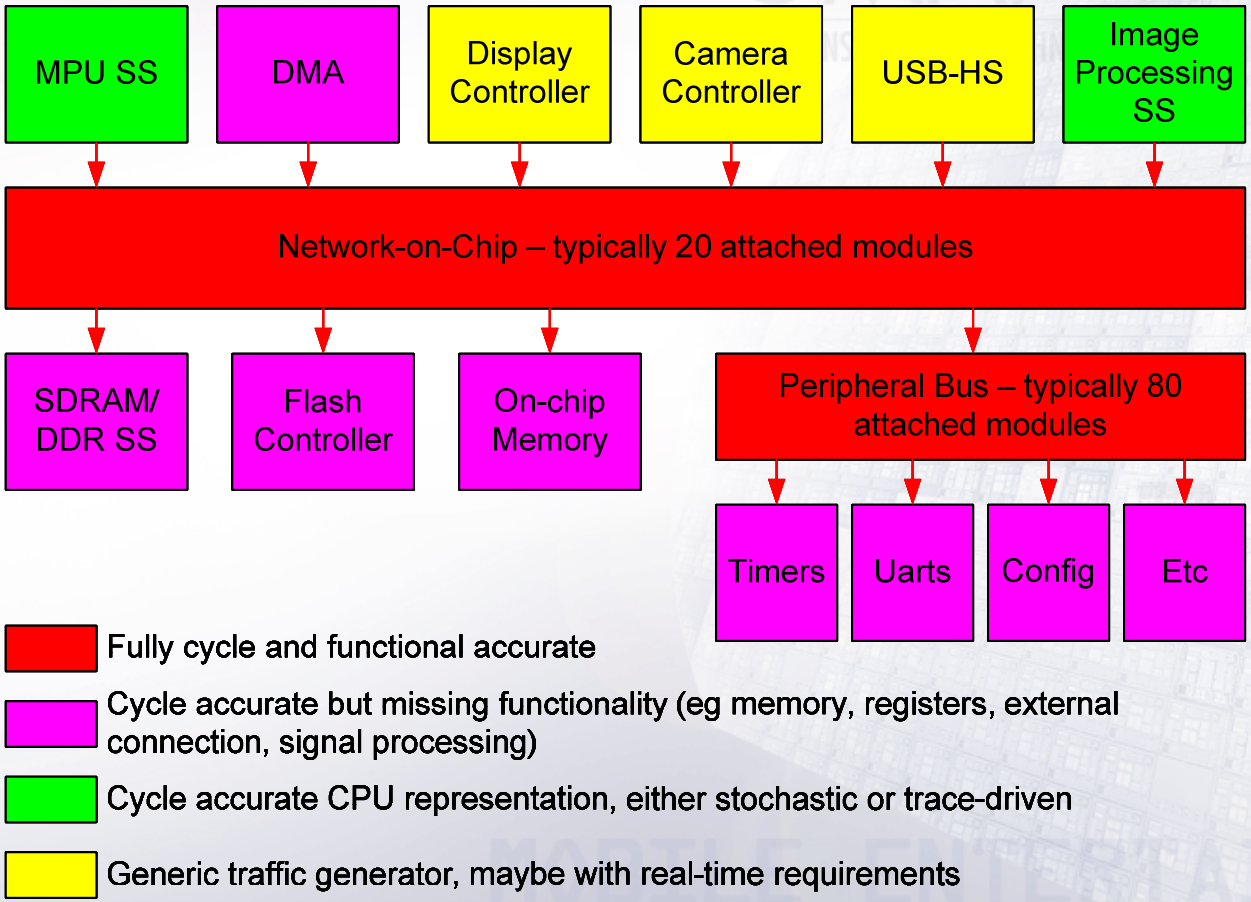
Why use OCP for OMAP-2?

- Single protocol
  - Single set of timing rules
  - Single set of validation tools
  - Easy to move IPs around in the system topology
- Standard protocol
  - Suppliers of third-party cores will support
  - Suppliers of EDA and validation IP will support
  - Widespread and therefore robust
- Powerful flexible scaleable protocol
  - OCP is configurable
  - Can meet the needs of high-end CPUs as well as simple peripherals
- Complete bus interface
  - Includes timing rules, DFT, etc.
  - Includes complete protocol-checking rules
  - *Includes comprehensive TLM infrastructure*

OMAP Modelling

- Architecture Modelling Team is both
  - Platform providers for modem/hybrid products
  - Platform users for ‘pure’ application processors
- We use ‘architecture-level modelling’ to
  - Extend and improve the OMAP2 platform
  - Optimise and validate all OMAP2-based products
    - 7 in development at the moment (ignoring simple derivatives)
    - Performance at SoC-integration level is our only concern
  - Support customer use of the products
    - Optimisation of use model
    - Feasibility testing of application/’phone designs

Typical SoC-Level Architecture Model



Use of OCP-IP SystemC TLM kit in SoC performance model

- All top-level bus interfaces are OCP-IP-TL1
  - Transaction-level modelling
    - Simplifies code development and testing
  - Cycle-accurate
    - Some interfaces must be modelled cycle-accurately
    - We want a single interface standard throughout
  - Mixture of accurate models of modules and ‘generic’ memories and traffic generators
    - OCP-IP TLM allows automatic adaptation of generic module behaviour to OCP configuration
  - Inbuilt monitoring
    - Every bus interface can be traced and/or protocol-checked
    - Every bus interface can provide latency and bandwidth stats

Requirements for the modelling activity

- Be well in advance of development (SW or HW)
- Be able to test proposed hardware changes
- Be able to react in hours to customer/product definition/bugfixer needing analysis of a new use case
- Provide *understanding* of behaviour
- Be comparable with RTL and silicon

EASE OF MODEL CREATION
EASE OF TEST CASE CREATION

Enablers:

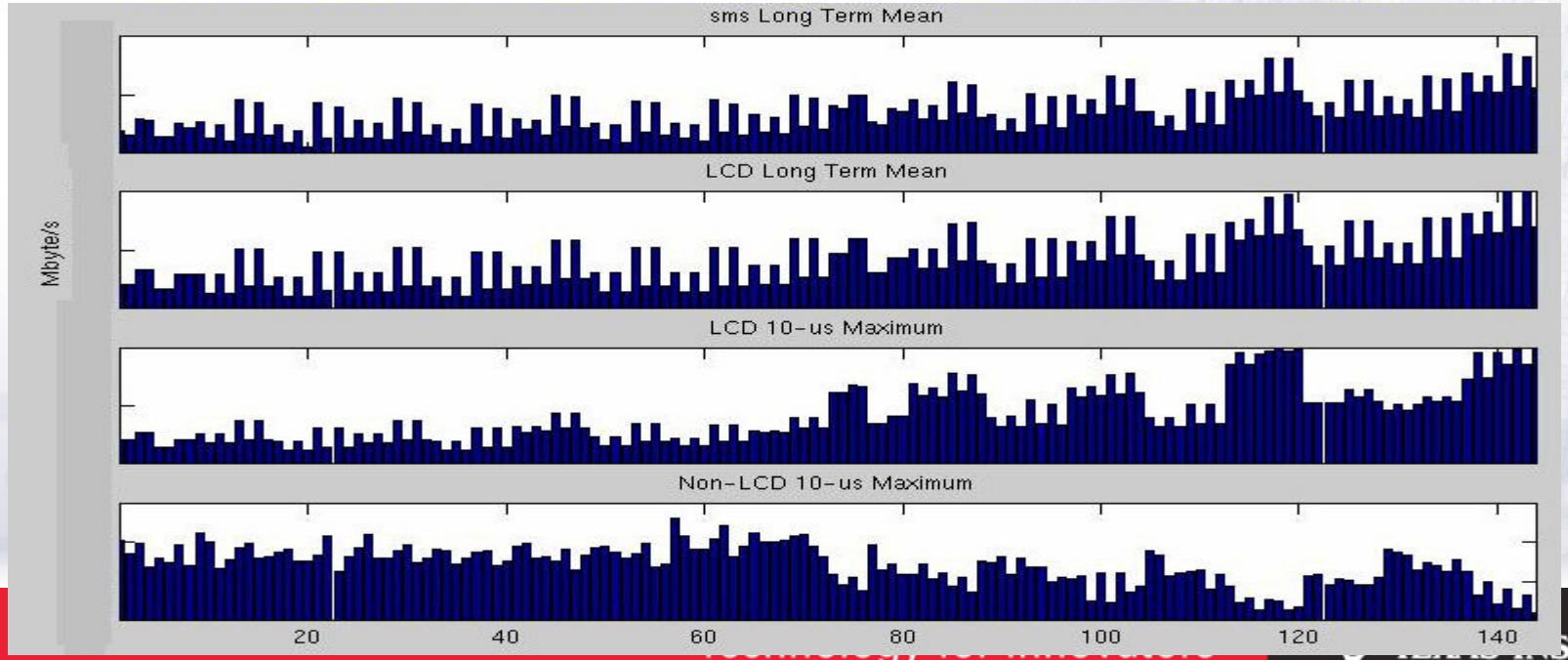
- Consistent use of one unique protocol: OCP
- Efficient high-level simulation language: SystemC
- Infrastructure supporting OCP in SystemC: OCP-IP TLM

EDA Support Requirements

- High-quality SystemC-aware C++ debugger
- OSCI-binary-compatible
  - Do not always have access to SystemC source code
  - Suppliers can not support multiple implementations of SystemC
  - Also need to specify OS and compiler-version
  - This is a general problem with SystemC: we hope that in the future a better solution will be found
- GUI
  - GUI for model assembly is not needed
    - Use a lot of conditional and multiple instantiation
    - Do not modify frequently top-level models
  - GUI for running test cases and viewing results
    - Low importance: mostly we work in batch mode
- Library of standard models
  - Registers, memories, bus interfaces, bus arbiters, etc..
  - Might be interesting, but need *standards* for interfacing with them first
  - So far we made our own
- Standards: Models *must* be EDA-vendor-independent

Only one results example: 144 different videoconference configurations

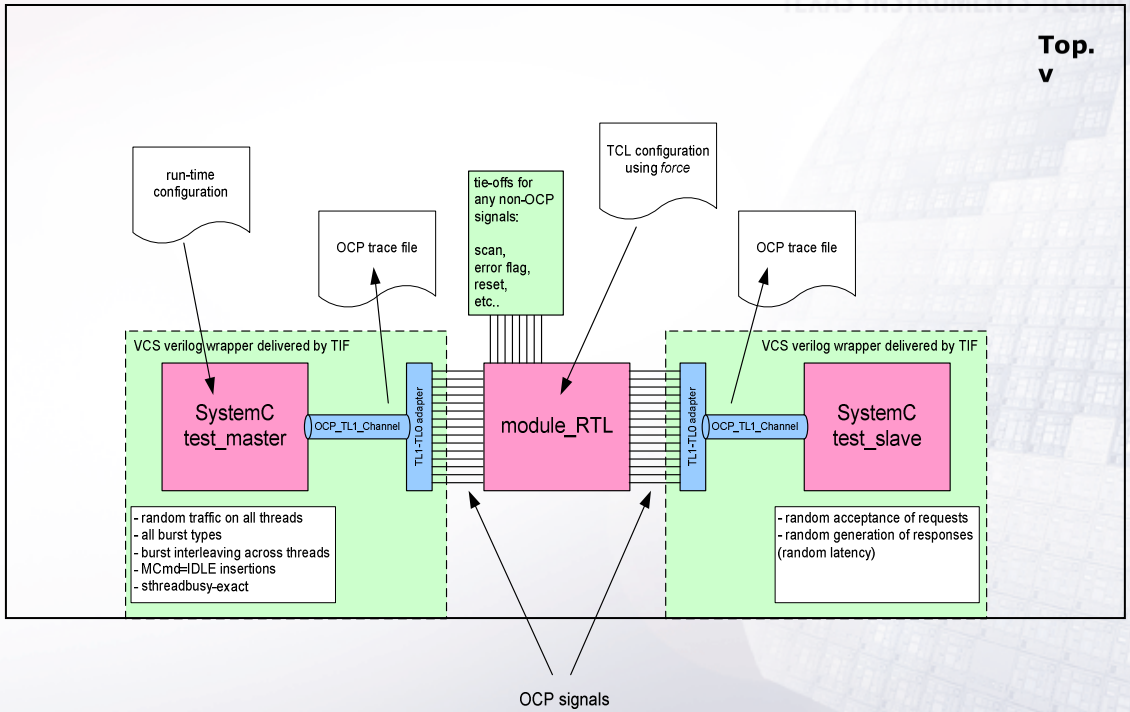
- Different screen sizes, orientations, frame rates, optimisation choices, etc, etc
- Results show:
  - Bandwidths and latencies (DRAM bandwidths for all test cases shown here)
  - Which cases pass
  - Behaviour in critical periods
  - Sensitivity of MPU to differences in other traffic
  - Lots of other goodies
- Measurements taken on OCP-IP-TL1 interfaces



Other levels of Abstraction

- OCP-IP Provides SystemC TLM Infrastructure
  - TL1: cycle-accurate TLM
  - TL2: cycle-approximate TLM OCP-specific
  - TL3: cycle-approximate TLM generic bus
- In OMAP
  - TL1 used as described above
  - TL1 used for validating accuracy of SystemC models against RTL implementation
  - TL3 used for very early studies dimensioning new products

RTL-SystemC Equivalence Testing



- Can run identical test case on RTL or SystemC-TLM model
- Uses OCP-IP TL1 Infrastructure
- Uses OCP-IP TL1-TL0 adapters
- Uses normal HDL simulator with native support for SystemC

Conclusions

- OMAP-2 is the technology behind the dominant force in mobile-telephone application processors
- Critical to SOC development are:
  - Reuse
  - Speed of assembly
  - Determinism of timing closure and back-end
  - Correct understanding of SOC performance before availability of RTL code or Software
- OCP is a key element in meeting these needs
- OCP-IP TLM/SystemC infrastructure is heavily used by TI for OMAP development and execution
- It works. It exists today.