

OCP-IP News

The Official Newsletter of the Open Core Protocol International Partnership

Membership Announcements

OCP-IP is proud to announce the following new members:

ActVision – designer of SoCs for multimedia applications including Mp3/WMA music and network video

Jetstream – developer of innovative silicon intellectual property (SIP) solutions

Silistix LTD – provider of on-chip interconnect networks that reduce design effort and provide lower power consumption

Temento Systems – provider of test platforms in the Electronic Design & Test Automation (EDTA) arena

Xilinx – developer, manufacturer and market promoter of advanced integrated circuits, software design tools and intellectual property

Industry Events

EDAC CEO Forecast

February 2, 2006
Hewlett-Packard
3000 Hanover St.
Palo Alto, CA

Design Automation and Test in Europe (DATE)

March 6-10, 2006
Messe Munchen
Munich, Germany

OCP-IP

Mission Statement:

Formed to promote and support OCP as the complete socket standard that ensures rapid creation and integration of interoperable virtual components.



By Ian Mackintosh
OCP-IP Chairman
and President

Letter from the President: Winning with Standards

2005 was a banner year for OCP-IP. Our Specification Working Group completed the formal release of OCP version 2.1 and a draft proposal for version 2.2 will be available early 2006. Our Functional Verification Working Group recently released a set of English language Compliance Checks which enables OCP compliance to be asserted in any chosen language.

The System Level Design Working Group recently released a SystemC Transaction Level Monitor (TLM) Channel version 2.1.1 along with a methodology white paper entitled, "OCP TLM for Architectural Modeling." New features in version 2.1.1 improve model interoperability, resulting in better productivity for system level modeling. We launched two new working groups; Cache Coherence and a Debug workgroup exploring OCP on-chip debug solutions.

The Marketing Working Group created a big splash with a major presence at the DATE 2005 Conference in Munich which include our first OCP-IP Pavilion; plans are underway for an even bigger event at DATE 2006. OCP-IP also had a plentiful year of presentations and articles; these are featured on our Web site and are available for viewing at www.ocpip.org/pressroom.

Our global expansion continued with new membership additions and Korean and Chinese language Web sites were added to our existing and well-trafficked English and Japanese Web areas. We finished the year strongly with the IP SoC tradeshow in Grenoble and multiple OCP training sessions in Beijing and Shanghai.

2005 was an extremely active and productive year. We thank everyone who had a hand in helping us promote and develop OCP and look forward to even greater success in 2006!

Sincerely,

Ian Mackintosh,
Chairman and President, OCP-IP

A DATE to Remember: OCP-IP Announces 2nd Annual DATE Pavilion

OCP-IP is excited to announce the 2nd annual OCP-IP DATE Pavilion, March 6-10 in Munich, Germany. The Pavilion is a "conference within a conference" and will host exhibits from several OCP-IP member companies including: CAST, Jeda Technologies, Nascentric, TransEDA, Sonics and Yogitech. The Pavilion is an open discussion forum in the midst of Europe's largest electronic system design exhibition. The program will combine expert panel sessions and papers, offering visitors a view of key technical trends and insight into the SoC market of the future.

Papers and panels will encompass the diverse issues surrounding re-usable IP, such as: IP development, purchasing, interconnect, verification and testing, IP quality, network on chip (NoC) and more.

Last year's Pavilion was an incredible success with high traffic and keen interest in the variety of presentations. Again this year, many prestigious industry leaders are scheduled to appear in our panel sessions.

OCP-IP members are encouraged to submit ideas for 2006 paper and panel topics to admin@ocpip.org.

We look forward to seeing you at DATE 2006 !

Working Groups: Reports and Updates

Specification Working Group

The Specification WG has reviewed the formal proposals supporting the agreed enhancement areas for the 2.2 specification, and is incorporating feedback from the WG into a draft version of the 2.2 specification, available to members in early 2006.

Technical Vision Working Group

The Technical Vision WG will meet in Q1 to fully re-examine and prioritize OCP-IP's role within the industry, reexamining our supporting infrastructure and benefits. The group has provided recommendations to all OCP-IP working groups and will work to incorporate their feedback in developing the final roadmaps for all work to be completed in 2006. This will then be submitted for approval by the Governing Steering Committee. The total set of deliverables coming available to OCP-IP members throughout 2006 will be particularly extensive.

System-Level Design Working Group

The System Level Design WG is developing the OCP SystemC TLM channel version 2.1.2. The new features include a new TL3 channel model and new access interface for connecting external instrumentation modules. A new set of abstraction layer adapters are being released for the latest channel, with full configurability. To improve design validation and verification, the SystemC assertion package is being released, based on the new standard Compliance Checks from the Functional Verification WG. Both releases will be available to members in January on the OCP-IP Web site.

Marketing Working Group

Throughout the past quarter the Marketing WG has attended numerous industry events including GSPx, IP SoC, and several events in China. Great attention has been given to preparations for the OCP-IP Pavilion at DATE 2006. For further details on the DATE Pavilion please see the article on the previous page. The Marketing WG also published an impressive insert in Chip Design magazine and released several press releases and articles regarding OCP-IP's continued growth.

Functional Verification Working Group

The Functional Verification WG has completed the OCP 2.1 protocol Compliance Checks. The public release version of this document is available to OCP-IP Members. The group plans to release a subsequent document (which includes functional coverage) for member release by Q1 2006.

Cache Coherence Working Group

The Coherence WG split the specification work into 3 parts, coherence model(s), interface signals/encodings and detailed examples. Of this the group has completed a first cut of the interface signals/encodings and is currently working on completing the coherence model description.

Debug Working Group

OCP-IP has granted an official charter to the Debug WG. This recognition already recognizes several months of encouraging work completed by the Debug study group. ■

University Corner



For more information visit
www.vdec.u-tokyo.ac.jp

and serves academia throughout Japan.

As an intellectual education and research center on VLSI technology, VDEC's mission is to educate students and provide support on VLSI chip fabrication for all academic organizations throughout Japan.

OCP-IP is pleased to welcome the VLSI Design and Education Center (VDEC), to the OCP-IP University community. VDEC, established in 1996, is headquartered in the University of Tokyo

VDEC performs various kinds of activities including exchange of VLSI design information as IPs, and provision of CAD software and licenses supporting chip design and fabrication.

Several different VLSI fabrication technologies, various CAD software, and testing facilities are provided through VDEC. Over 450 research groups from over 150 universities in Japan are utilizing the services and support of VDEC.

The addition of VDEC to our membership roster enhances the academic support that OCP-IP has already established in its University Program. ■

Better Products, Happier Customers with Current-Based Simulation/Verification and the Open Core Protocol

By Dr. Ramon Acosta, Nascentric, Inc



For more information visit www.nascentric.com

The demand to deliver faster, smaller, portable and more powerful wireless products is what drives the electronics market. Every visit to the local electronics store surprises us with a plethora of consumer electronics that change the way we live and communicate. Portable home healthcare electronics include a wearable non-invasive glucose monitor for diabetics, an in-home hemodialysis unit, and do-it-yourself screening tests for conditions ranging from high cholesterol to blood-borne infections. Today's cell phones offer movie downloads and remote programming of home electronics that allow consumers to record television shows. To be successful in the marketplace, these mobile devices must match consumer demands. They must have many technically advanced features, perform instantaneously and be extremely small and inexpensive.

Satisfying these demands constantly impacts engineering schedules, strains limited engineering resources and interjects unpredictable costs into development budgets. To accelerate engineering schedules, minimize engineering resources and better manage development costs, many semiconductor manufacturers integrate third-party IP into their designs. The availability of robust IP alleviates a significant amount of pressure from the design teams; and its extensive usage in today's large SoCs is a standing testament to its industry-wide appeal.

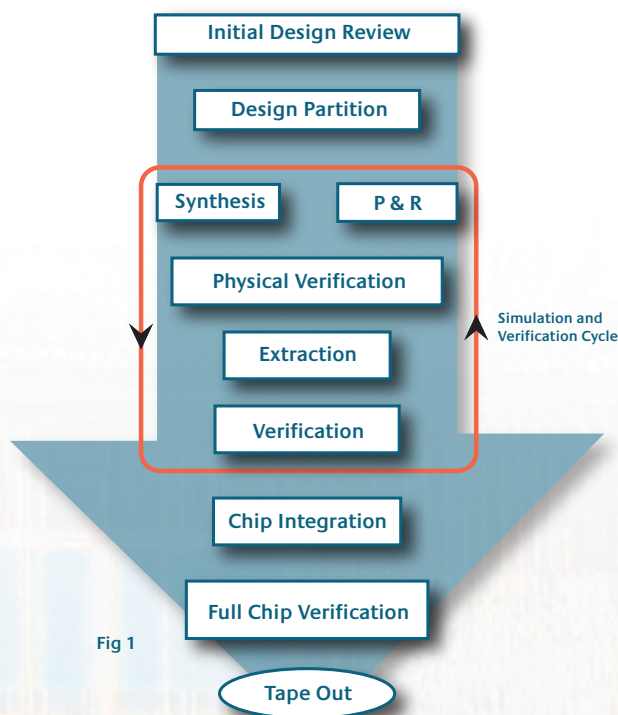
However, the close interaction between blocks in large SoCs makes it absolutely necessary to test functionally in each of the blocks separately while ensuring that these blocks interoperate flawlessly when connected.

The functional interaction between the interfaces is complex at best, requiring lengthy verification tests.

IP blocks purchased from third-party vendors often need to be verified within the entire context of the chip rather late in the design cycle. Limited verification resources frequently inhibit the design teams ability to perform the comprehensive simulation and verification that is crucial for silicon success. In the midst of this new complexity, the chip integration team may not be aware of the intricacies of some blocks and may miss some small, yet crucial, functionality tests.

To address some of these issues, the industry generally employs two methodologies for the design of large and complex chips; top-down and bottom-up.

Top-Down Design Methodology



Top-Down Methodology

The more prevalent methodology of the two is the top-down approach (see Fig. 1). The tools supporting this design flow are robust, mature, highly automated and the issues are well understood. Commonly referred to as "Big D, Little a" designs, these architecture-driven designs mainly include digital blocks with a small amount of analog content. Designers using this methodology are familiar with HDLs such as Verilog and VHDL, and are comfortable using them in their design.

These designers generally focus on the functional view and do not concern themselves with a SPICE-level view of the analog block. A well-defined interface, such as the Open Core Protocol (OCP), helps

them integrate the digital side IP blocks into the larger design. This methodology provides greater accommodation for changes to the design specification later in the design cycle. Proponents of this methodology then require a fast, high capacity, mixed-signal simulator to help functionally verify the digital/analog interface.

Bottom-Up Methodology

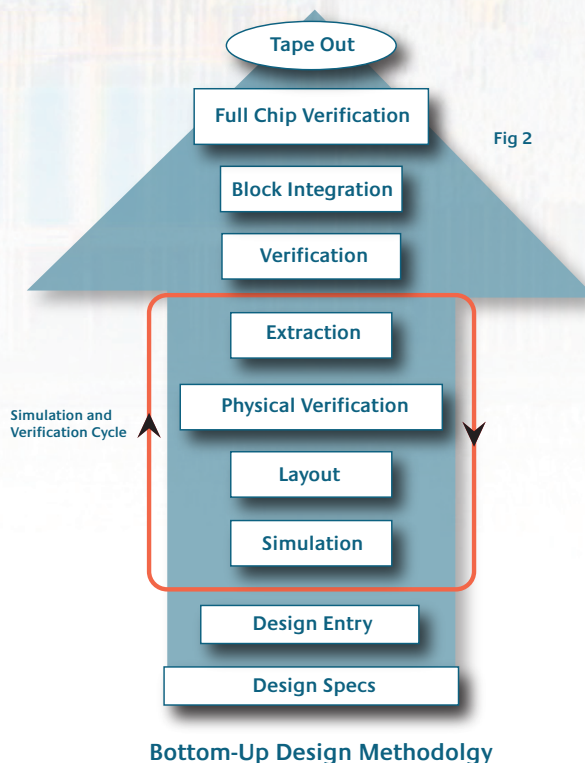
With the increase of mixed signal content in SoC designs, the bottom-up methodology (see Fig. 2) is becoming more prominent. These designs are typically block-driven “Big A, Little d” designs. While there are very mature point-tools, the design flow itself is very patchy and the level of integration is poor. Issues with the digital/analog blocks are quite complex and have more frequent analog content. Designers are very familiar with the SPICE-level view of the functional block yet they remain highly skeptical of any abstraction above the SPICE level. The functionality of designs is tested at every stage of the design cycle and when a problem is encountered at the top level, the integration/design team is typically responsible for diagnosing and fixing the problem.

Design teams adopt popular formats such as OCP to help seamlessly integrate their IP blocks. The design cycles for bottom-up methodologies tend to be long and rather inflexible to accommodating design specification changes late in the development cycle. In this case, designers require a fast, accurate mixed-signal simulator to help simulate large designs with greater accuracy.

Each of these methodologies provide significant structure to design teams but their successes are still dependent on the specifics of the design adoption. It is apparent that the availability of a fast, accurate, high-capacity, mixed-signal simulator remains a critical factor for success in either methodology. Design and verification teams have stoically employed traditional SPICE and Fast SPICE solutions to address their needs for these mixed signal designs. However, this approach has worked well for small functional ana-

log and digital blocks, but fails for larger scale mixed-signal designs. There are several reasons for this:

- The traditional SPICE and Fast SPICE solutions primarily use voltage-based device models to predict the behavior of analog circuits. This works well for small stand-alone designs since the requirements on simulation capacity are small and performance is not as critical. Using a similar approach proves to be highly inefficient for large mixed-signal designs.
- The move to nanometer processes has introduced several physical effects that require a better understanding of the current flow through critical nodes. Traditional SPICE and Fast SPICE engines can determine this value, but only at great computational expense or by compromising accuracy.
- The traditional solutions employ one or two type(s) of simulation engine(s). As mixed-signal designs have multiple functional blocks with unique circuit and interconnect behavior, the 1 (or 2) simulation engine approach severely limits the performance and accuracy.
- When using SPICE/Fast SPICE solutions with voltage-based models, designers are given the option of either accuracy OR performance. This has proven to be a barrier for mixed-signal designers whose analog IP blocks require-greater simulation accuracy; whereas digital blocks need better performance and larger capacity. Since both blocks need to be simulated together the trade-off presents a ‘no-win’ selection.
- The nature of the mixed-signal blocks requires multiple concurrent analyses (such as detailed power analysis, grid analysis, etc.) to be performed while still checking for functionality and timing. Existing SPICE/Fast SPICE solutions are either too limited on capacity or too inaccurate to perform these types of functionality checks.



These issues have been long since noted throughout the analog IP/ mixed-signal design community which has clamored for a next generation simulation/verification solution for mixed-signal SOC designs for some time. To create a next-generation Fast SPICE

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Addition of Tagging to the MIPS 24K Core using OCP 2.1

By Sanjay Vishin, MIPS Technologies



For more information
visit www.mips.com

Introduction:

MIPS has embraced an open standards philosophy while designing the 24K [1] processor core. MIPS decided to move the main memory interface to a forward looking, non-proprietary open standards-based on-chip protocol, Open Core Protocol (OCP). The OCP was at revision 2.0 when the 24K processor core was being developed. One reason OCP was chosen, was its independence from the physical transport which provided scalability in performance. This feature was important to MIPS as MIPS processors are known for their scalable performance and are used in a variety of applications including many high performance processors (set-top boxes, network infrastructure etc.). In addition to the applications, scalability of interconnect and requirements for the next generation of deep sub-micron geometries were important to consider. OCP's layered interconnect specification met MIPS needs well, except for one caveat.

Problem:

For high performance, the OCP 2.0 Specification provides 'threads' which a designer can use to send multiple independent transactions on the same set of wires. This is very useful for certain agents including multi-channel DMA cores which multiplex many independent channels on to a physical OCP port. However, MIPS needs were slightly different; they wanted a high performance out-of-order data return mechanism (The 24K processor can handle out of order responses) with the least area cost penalty, in effect, a lighter mechanism than threads. The complete channel separation of threads and the associated penalty due to independent flow control for each thread, was not optimum for MIPS' needs. The obvious solution of mapping tags to threads did not work well as threads are completely independent and would require the addition of logic to the processor core in order to resolve memory hazards occurring between threads. For example, a load and a store mapped to multiple threads could carry the same target address. Since threads do not guarantee any order between them, the load could return the value of memory before or after the store; resulting in a hazard. MIPS decided to work with the OCP-IP Specification Working Group (SWG) and help define a 'Tagging' extension to OCP-IP version 2.0. This was the main extension to the specification when the version was released as OCP 2.1.

Solution:

The new construct added in OCP 2.1, tags, are a lighter¹ mechanism as compared to threads; they share the same flow control and buffering between them, resulting in a low implementation cost in both the processor as well as the interconnect. With OCP 2.1,

it is conceivable to have a system which has a mix of threads as well as tags. Tags and threads have a hierarchical relationship; tags exist within a thread. So an interface with 4 threads and 4 tags per thread, has the ability to keep 16 outstanding transactions at the interface. This interface can have 4 sets of flow control signals, one for each thread. The 4 tags within each of the 4 threads will share the flow control assigned to the thread in which they exist. Without tagging we would have 16 sets of flow control signals and the interconnect would have to keep 16 sets of buffers at each link entrance/exit². With tagging, the storage requirements in the interconnect are substantially reduced (by a factor of 4 in this example).

Tagging allows the 24K³ processor to accept responses out of order and take full advantage of a hierarchical memory system. A hierarchical system is composed of multi-banked DRAMs and level 2 (or higher, i.e. level 3 caches etc.) caches where the return data response depends on hits in the level 2 (or higher) cache, or hits in an open page of a DRAM. It is also possible to retire a write out of order with respect to the request order of the write with tags, although the performance gains expected may not be as much as for returning read responses out of order. Further, tagged responses can only be re-ordered if they are not directed overlapping addresses, which was a requirement for 24K. The 24K processor can keep 6 transactions outstanding and so uses a 3 bit tag. Each outstanding transaction is allocated a buffer in the 24K before it is issued on to the OCP interface. This implies that the processor can absorb all outstanding responses even if they are all out of order, which is a must for a deadlock-free implementation.

Conclusion:

Tagging is a new tool for SoC designers to build lean high performance systems with OCP 2.1. By integrating tags hierarchically within threads with a common flow control mechanism, tags retain the powerful deadlock free properties of OCP 2.0⁴. As OCP 2.1 IP cores become more common we expect more systems will be built with tags or with mixed threaded and tagged interfaces. ■

¹ Lighter^{*} in terms of Area.

² The extra overhead for tags in the interconnect is basically storage for the tag identifiers, while for threads its buffer storage (which tend to be larger) along with thread identifier storage.

³ Besides tagging some other extensions to MReqInfo and MAddrSpace were carried out in order to support cache management instructions and a strong synchronization operation, but our focus here is on tagging.

⁴ Tags are pure data labels with no dynamic property which makes them safe from a deadlock point of view. This is a nice property which other on-chip point to point interface standards do not possess.

References:

[1] http://www.mips.com/content/Products/Cores/32-BitCores/MIPS3224K/ProductCatalog/P_MIPS3224KFamily/productBrief

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simulation and verification solution one must begin by thinking out of the box. For example, Nascentric's Nascim is a significant departure from the traditional SPICE and Fast SPICE approach to simulation, as it adopts a current-based transistor and interconnect model approach. The basic presumption is that active MOS devices are current-based devices, rather than voltage-based. By adopting the current-based approach, Nascim overcomes the key short-comings of traditional voltage-based solutions and provides a fast, accurate, high capacity simulation and verification capability. Additionally, it features innovative schemes that accurately capture the complex interconnect behavior and account for the greater part of signal loading. Multiple dedicated simulation engines combined with intelligent event-based simulation will accelerate the simulation/verification time. Customer trials have demonstrated speed-ups of 2X-10X run time improvements as compared with existing Fast-SPICE simulation and verification solutions while maintaining equal or better accuracy.

Successful development and implementation of third party IP is integral to meeting a design's feature, schedule, performance, size and cost objectives. Adopting standards such as OCP are paramount in integrating verified combination of analog and digital blocks. Implementation of the IP blocks needs a strong foundation integration standard and requires that boundary conditions be well understood and fully characterized. By performing simulations more quickly and ensuring more robust verification coverage, next-generation simulation solutions will bring relief from much of the pain currently experienced in older simulation and verification approaches. ■

Dr. Ramon Acosta, V.P. of Engineering at Nascentric, is guiding the development Nascim, the next-generation Fast SPICE simulation tool. For additional questions, please contact the author: Ramon.Acosta@Nascentric.com

2005 Contributor of Year

OCP-IP was pleased to announce a joint Contributor of the Year award to CoWare and MIPS Technologies. The Award is given each year by the OCP-IP Governing Steering Committee to a member or members who have made key contributions to the further advancement of the OCP specification or surrounding infrastructure.



MIPS Technologies is recognized for its work in the OCP-IP Specification Working Group;

in particular for its contributions in the area of out-of-order tagging. Tagging provides the ability for interconnect and targets to re-order transactions for non-conflicting memory addresses within a single thread. Unlike threads, which enforce no ordering restrictions, tagged transactions ensure that read/write hazards are respected by the system. Tagged transactions are particularly attractive for advanced embedded CPU architectures, like the MIPS32[®] 24K[®] processor core family, which can exploit the parallelism offered by out-of-order transaction processing, but require consistent memory ordering.



MIPS recipients are John Bourgooin, CEO (Left) and Sanjay Vishin, System/SoC Architect (Right).



CoWare was acknowledged for contributions in the OCP-IP System Level Design Working Group. The

company made key contributions to the development of the SystemC Transaction Level Modeling (TLM) Channel version 2.1.1 and the methodology white paper, OCP TLM for Architectural Modeling. The new features in version 2.1.1 improve model interoperability, resulting in better productivity in system level modeling.



CoWare award recipients are Eshel Haritan, Vice President of Engineering (Left), Tim Kogel, Sr. Staff Research Engineer (Center), and Karl Van Rompaey, Chief Technical Officer (Right). ■

We sincerely thank both CoWare and MIPS for their contributions to OCP-IP!

Recent Publications

Available in the OCP-IP Press Room at
www.ocpip.org/pressroom

Press Releases

November 8, 2005: Temento Systems Joins OCP-IP

November 1, 2005: Jetstream Media Technologies Joins OCP-IP

October 25, 2005: OCP-IP Releases English Language Compliance Checks

October 24, 2005: Mercury Computer Systems Joins Xilinx Corporation in Open Core Protocol International Partnership

Articles

December 12, 2005: Video Effects IP Core For Hi-Def DVD Recorders, Camcorders and Set Tops Speeds Design With OCP Interfaces - *VI DesignLine*

December 12, 2005: OCP-based Memory Access Arbitration For a Digital Sampling Oscilloscope - *Design & Reuse*

December 6, 2005: OCP Is One For Me - *PLDesignline*

November, 2005: OMAP 2420 Antes Up For Handsets - *EE Times*

November 28, 2005: Use OCP Interface Technology in SIPs for Video Coding - *Design and Reuse*

October 31, 2005: SoC Design Success: Winning with Standards - *HWS World*

October 17, 2005: OCP Interface for SoC - Verifying the Implementation of Embedded Processors - *Design and Reuse*

Announcements

2.1.2 SystemC Models – Available early 2006

The System Level Design WG is preparing for the release of the OCP SystemC TLM channel version 2.1.2. The new features include a new TL3 channel model and new access interface for connecting external instrumentation modules. A new set of abstraction layer adapters will be released for the latest channel, with full configurability. Check the OCP-IP Member's area for further updates.

OCP CoreCreator 4.0 Training Now Available

The OCP training for CoreCreator 4.0 is now available to OCP-IP members. To request a CD of this training please contact admin@ocpip.org.

OCP 2.1 Training – Now Available

Training for the OCP 2.1 Specification is now available to OCP-IP members. To request a CD of this training please contact admin@ocpip.org.

OCP 2.1 Training – Now Available in Japanese!

OCP 2.0 training in Japanese is now available to OCP-IP members. If you would like to receive a free copy, please send your request to admin@ocpip.org. Please remember to include your complete shipping information with your request.

OCP Technical Support – Now Available in Japanese!

OCP technical questions in Japanese can now be accepted by e-mailing jpotech@ocpip.org.

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