Volume 1 Issue 1
October 2002

OCP-IP News

The Official Newsletter of the Open Core Protocol International Partnership

Membership Announcements

OCP-IP is proud to announce the following recent members:

Amphion Semiconductor—A provider of semiconductor Intellectual Property (IP) for digital video and broadband wireless System-on-Chip (SoC) design.

Broadcom—A provider of highly integrated silicon solutions that enable broadband communications and networking of voice, video and data services.

CAST—A provider of a broad line of general-purpose IP cores for FPGAs and other applications including 8- and 16-bit processors, peripherals, buses, network interfaces, communications devices, multimedia operations and encryption functions.

Duolog—A provider of IC and software design services.

Prosilog—A developer of new tools to help system architects and software and hardware engineers to design complex, digital, analog or mixed electronic systems for integration in next-generation components.

QThink—A provider of cutting-edge chip design services and solutions to clients in a variety of product sectors.

Siroyan—A designer of high-performance, scalable DSP IP cores.

TranSwitch—A provider of high-speed VLSI solutions—microchips—which enable communication more readily, affordably and reliably via voice, fax, e-mail and multimedia.

Verisity—A provider of proprietary technologies and software products used to efficiently verify designs of electronic systems and complex integrated circuits.

Virtual IP Group—A provider of IP development, licensing and integration services as well as front-end and back-end design services including firmware development for embedded system solutions.

Virtual Silicon—A supplier of semiconductor IP and process technology to manufacturers and designers of complex SoC.

Industry Events

FSA Suppliers Expo

October 3, 2002
Santa Clara, California

SoC for a Connected World and IP Based SoC Design

October 30-31, 2002
Grenoble, France

Tentative Events

DesignCon

January 27-30, 2003
Santa Clara, California

Electronic Design Fair (Far East)

January 30-31, 2003
Yokohama, Japan

DATE (Europe)

March 2003
Munich, Germany

Mission Statement:
Formed to promote and support OCP as the complete socket standard that ensures rapid creation and integration of interoperable virtual components.

Letter From the President

Welcome to the first edition of the OCP-IP newsletter. The purpose of the newsletter is to provide members with one convenient place in which to find all OCP-IP updates and information.

We continue to be amazed by the attention and interest we receive. The organization continues to see a solid rate of growth, and we believe that validates the need for a well-supported universal socket. Our most recent achievements include securing several new members, dramatic progress in our technical working groups and several additions to our website. You will find more details on each of these topics throughout the newsletter.

We hope you find this format useful and convenient, however, we are always looking for ways to improve. If you have any questions or suggestions on how we can better the newsletter to meet your needs, please send us a message at admin@ocpip.org.

Sincerely,

Ian Mackintosh

Ian Mackintosh
President, OCP-IP

Working Groups: Reports and Updates

Functional Verification

The Verification Working Group meets on a regular basis and is making great progress. While entertaining discussions with various bodies, it is also evaluating various formal and functional verification alternatives.

Specification and Memory Semantics

These working groups have made tremendous progress over the last few months and have completed the proposals for enhancements in the 2003 version of OCP. The new version of OCP is scheduled for release in early 2003, and the enhancements include:

- A model for write transfers—provides for precise end-to-end-responses
- Enhanced burst model—provides both burst length and packet style transfers
- Support for specification endianness
- Support for user-defined in band command data and response extensions
- A proposal for even lighter weight OCP interfaces with read only/write only/FIFO style IP cores
- Support for lazy memory synchronization

Marketing

The Marketing Working Group (MWG) is extremely pleased with its progress. The group has been incredibly busy ensuring the on-time publication of press releases and articles as well as managing the logistics for all trade shows.

This year, the MWG has sent out seven press releases to announce just a few new OCP-IP members. It has secured more than 20 articles in both U.S. and European press. To view all press releases and articles, visit www.ocpip.org

The MWG is encouraged by the amount of interest it has seen at trade shows. This is a clear indication of the need for an open industry standard and a well-supported universal socket that frees companies from the constraints of a unique application. The MWG expects to see this increase of interest to continue and is excited at the opportunities future trade shows present.

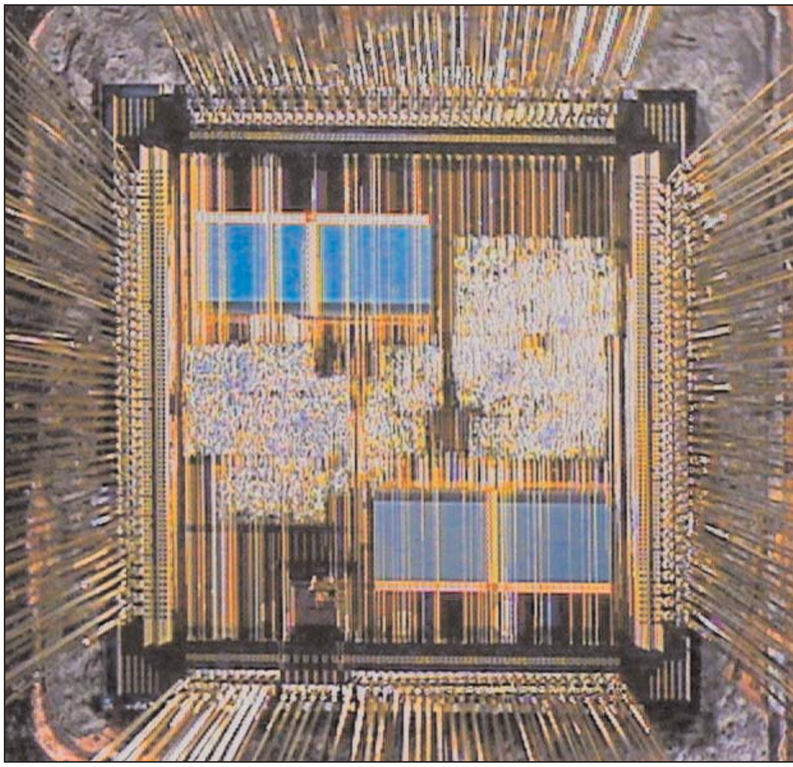
Look for more key announcements in press releases and articles in the coming months. ■

The Importance of Sockets in SoC Design

Semiconductor fabrication advances and escalating market pressures have made time-to-market and design reuse continuing topics within the semiconductor industry. It is clear that decreasing an SoC's development time can simultaneously decrease time-to-market. The design reuse practice is similarly simple and understandable – design once, reuse many, many times.

The solution to maximizing core reuse potential requires adopting a well-conceived and specified core-centric protocol as the native core interface. By selecting an adopted industry standard, core designers not only enable core reuse for cores developed within their own enterprise, they also enable reuse outside the enterprise under Intellectual Property (IP) licensing agreements.

OCP is the only complete and fully supported socket in the SoC design industry. The growth in our membership clearly shows the support in the SoC community for our independent industry standard that makes design reuse a reality. ■



On the Web for Members Only

Recently, we have made several enhancements to the "Members Only" section of the OCP-IP website. The additions include new working group information as well as an OCP template and confidentiality page. Members of OCP-IP can make suggestions for improvements to the "Members Only" section by sending an email to admin@ocpip.org. ■

Specification Announcements

Proposals for enhancements to the 2003 version of OCP have been completed. The new version is expected to be available in the early months of the coming year. ■

Featured Member: Siroyan

Understanding the benefits to the SoC design industry from the use of the only complete and fully supported (OCP) socket and the first truly open industry standard, Siroyan became a Sponsor Member of OCP-IP in September 2002.

Siroyan will use OCP in its current and future generations of DSP cores and use wrappers for each targeted bus.

As a Sponsor Member of OCP-IP, Siroyan can take an active role in the partnership's working groups and participate in developing future enhancements for OCP. (For an update on working group activity, please see Working Groups: Reports and Updates section on page 2.)

Siroyan is headquartered in Reading, UK and employs some 50 technical and commercial staff at its headquarters and design centers. ■

Standard Socket Interface Tapped

By Pete Cumming
Architecture/SoC Manager, Wireless Terminals Business Unit
Texas Instruments Inc., Dallas, Texas
Reprinted from the September 9, 2002 issue of EETimes, permission from CMP Publications

Emerging 2.5G/3G wireless markets are introducing new data types and application performance requirements into the handheld-terminal market. But the market promises to be so dynamic that a new level of design flexibility will be required as well. Not only do we need to be able to move new internally developed Intellectual Property (IP) into system-level chips rapidly, but our partners, handset and PDA manufacturers such as Nokia, Ericsson, Sony, Sendo, HTC and Palm, need a way to incorporate their own IP with equal facility.

These needs have led our engineers to develop a platform architecture with a standard socket interface. The development has been an evolution based on a decade of wireless experience and on innovations in open socket thinking.

An example of this platform, the Open Multimedia Applications Platform (OMAP1510), meets multimedia design requirements optimally through a two-core approach.

The definition and development of the first-generation OMAP products were based on more than 10 years of wireless-system expertise. Devices prior to the current OMAP products had the same power, area and time-to-market constraints we see today, and we developed IP and interface standards to support these goals. In particular, we used in-house bus standards. We refer to Level 3, or L3, in contrast to a Level 2 cache and peripheral (Level 4, or L4) levels of the bus hierarchy.

First-generation OMAP devices successfully reused much of the technology from these previous designs and were based almost exclusively on TI-developed components. However, it is natural that we changed how we build OMAP devices as silicon capability, design methodologies and the IP market matured.

Our first-generation bus standard, known as Rhea or TIPB, epitomizes the bespoke, bus-based approach that was common in first-generation System-on-Chip (SoC) designs. We developed a bus that made use of extensive clock gating and variable data widths to minimize power and area. The approach was successful in these goals, and a library of standard components supported asynchronous peripherals. This approach, however, had a number of problems that became more serious as we designed more peripherals, performed more integrations and wanted to use more advanced electronic design-automation tools and methodologies.

Additionally, using an in-house standard made it hard for us to exchange IP with our customers — importing modules from them was difficult and providing modules for their ASICs was equally difficult, except when they made use of our bus. Finally, there were some modules that we wanted to use as L4 components in some devices and as L3 components in others, while other modules such as bridges and DMA had to talk to both. The lack of synergy in the two bus/interface standards made this difficult.

To deal with these issues, we introduced the Open Core Protocol initially as a standard for the design of IP (see www.ocpip.org for the OCP specification). Our team chose OCP after a lengthy evaluation of the available options and after making our choice, we assigned experienced engineers to ensure the adoption was successful throughout the TI peripheral design community.

The first step in adoption was to use OCP modules in a legacy environment. Despite the fact that we did this first in a complex device designed under significant schedule pressure, it was a relatively painless process. Subsequent devices are native OCP throughout and this has allowed us to significantly simplify the peripheral architecture of OMAP devices. Integrating modules with legacy interfaces into this native environment is also possible, although modules are being migrated quickly, so that this is not a major part of our next-generation designs.

Adopting an industry-standard interface has made integration of customer-provided modules much more straightforward. Even those modules designed with legacy interfaces can be easily integrated by bridging to OCP and connecting to

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Socket Interface Tapped (continued from page 4)

a standard socket. Similarly, our customers — whether or not they have adopted OCP themselves — find it convenient to receive OCP modules from us since we or they can easily provide a gasket to their chosen interconnect.

Our initial designs were based on an optimized “traffic controller” that included critical memory controllers (static DRAM, execute-in-place NOR flash) as well as the interconnect network. This interfaced to the ARM processor and DSP via the processor’s own interfaces and to other initiators such as direct memory access (DMA) through a simple 32-bit in-house interface.

We built the first OMAP devices around a core hard macro — known in TI’s ASIC flow as a subchip — so as to reuse the investment in the traffic controller and its related components. The subchip included various expansion ports intended for on- or off-chip devices. Again, these ports used in-house interfaces intended to match the intended uses.

Over the various generations of OMAP development, we have found that some of the clock-cycle constraints have become less severe since memory speed has not kept up with our digital process development. In addition, the expansion ports have been used for applications other than those that we intended.

This has led to a gradual migration of the design style so that today we are in a position to standardize on the OCP socket interface. We are using this socket not only for interfaces to the core of processors and memory interfaces, but also within it.

Unfortunately, we cannot move entirely to native interfaces since some IP is not yet available with our chosen interface. However, knowing that this would probably be the case, we chose our socket standard to allow maximum cooperation with other standards in order to bridge devices to our OCP environment.

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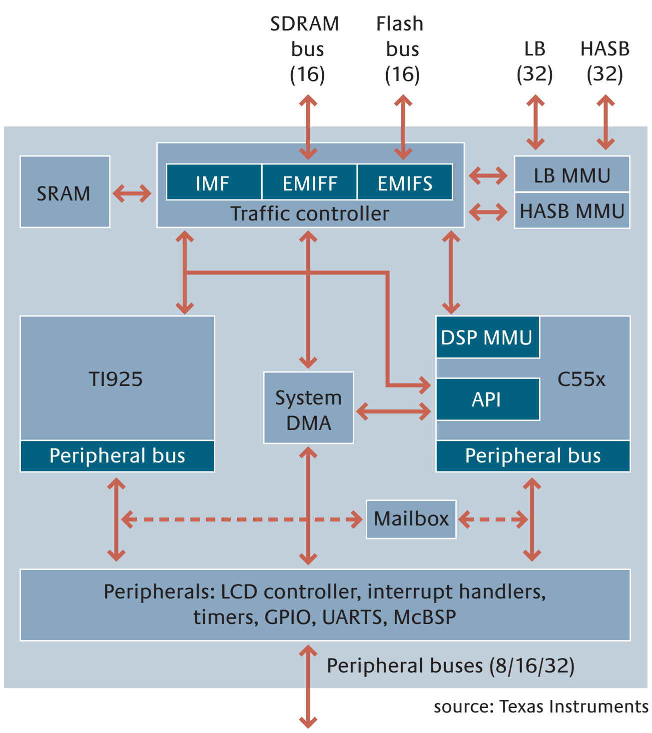
Open Multimedia Applications Platform



source: Texas Instruments

GPP
TI925 core

- 16 kbytes 1-cache
- 8 kbytes D-cache
- Write buffer
- I-MMU and D-MMU
- Dual TLB

DSP
C55x core

Internal Memory
- 48 kW SARAM
- 32 kW DARAM
- 16 kW PDROM

24 kbytes I-cache
Graphics hardware accelerator
ARM port interface

IPC

- Mail boxes
- API
- DSP MMU

System DMA
Traffic controller
Internal SRAM
Buses
Peripherals

The Open Multimedia Applications Platform (OMAP) 1510 processor meets multimedia design requirements through a two-core approach. Open Core Protocol (OCP) has allowed designers to simplify the peripheral architecture of OMAP devices. Designers also found it easy to bridge OCP to other interfaces and to fashion a design with interfaces that fit naturally into their blocks.

Socket-Centric IP Core Interface Maximizes IP Applications

Semiconductor Intellectual Property (IP) designers strive to ensure their IP can be utilized by the widest possible range of applications to ensure maximum return on their engineering investment. However, the common older practice of supporting a bus-centric protocol as an IP core's native interface ultimately limits the market into which an IP core can subsequently be utilized or sold. Fortunately, there is now an optimized and fully-supported interface approach available that utilizes the benefits of the OCP SOCKET.

Bus protocols are based upon traditional printed circuit board styles of interconnect structures that consist of hierarchical wire bundles and are proving to be ineffective for System-on-Chip (SoC) designs. All bus protocols rigidly define an inter-block dataflow communication methodology and demand the use of this signaling style to the exclusion of any other technique. Also, sideband control and test signals are not typically supported by computer-bus style protocols and require the system integrator to deal with them in an ad hoc way for each system design. This means that if an IP designer inflicts a particular bus protocol upon his IP core, reuse with a different bus protocol may only be possible via the loss of features or performance, or may not be possible at all.

The solution to maximizing an IP core's potential reuse, and realizing the advantages leveraged by proven industry standards, is to adopt a well-specified core-centric protocol as the IP's native interface. A comprehensive and scalable interface specification between IP cores and on-chip interconnect systems allows IP core developers to focus on core generation without having to know any details about the end-systems in which a core might be eventually utilized, nor anything about the other IP cores that might be a part of those end applications. Essentially, the problem is best solved with the use of a complete and fully supported SOCKET.

With this socket-based approach, system integrators benefit by not having to deal with an unending series of unique core protocols and delivery styles. The use of standard IP core interfaces eliminates having to repeatedly adapt each core in preparation for each SoC integration, and instead allows the system integrator to focus on system level design issues. Also, since standard interfaces decouple the cores from the on-chip interconnect and from each other, it is simple to change out one core for another to better meet changing system requirements.

For an IP core to be truly reusable, it must remain untouched as it moves from system to system. A core's interface must represent the unchanging requirements of the core, rather than the continuously differing requirements of each system's interconnect. A core need not be re-adapted every time the bus width, frequency or electrical loading changes if a complete socket is specified.

Since core interface requirements are as diverse as the IP cores themselves, there is no rigid one-size-fits-all interface. A standard core interface specification must be scalable and configurable to adapt to the wide range of requirements. It is also not sufficient for an interface specification to only capture dataflow signaling. It is important that all signaling between a core and the system are captured. Non-dataflow control signals (such as interrupts, error signals and flow-control signals) and test signals (used for debug

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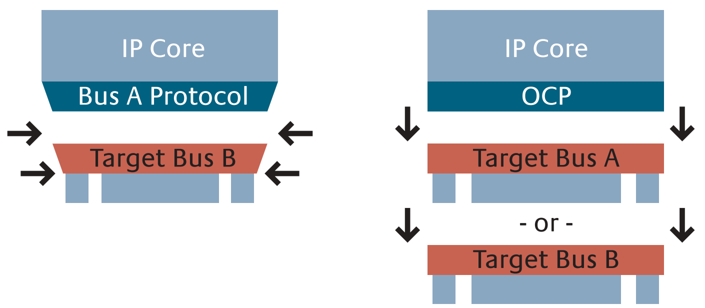
Core-Centric vs. Bus-Centric



Bus-Centric Protocol Interfaces:

- Bus configuration assumptions for a native interface limit IP Core features–AND–eliminate or limit capabilities in successive bus structures
- Do not address ALL core communication
- Sideband Control and Core Test are not addressed

OCP is a Core-Centric Protocol:

- Facilitates unrestricted delivery of ALL core signals and features
- Enables unconstrained interface bridge to ANY bus structure

and test of the completed chip) are typically ignored or incomplete, except for the OCP.

The freely available Open Core Protocol (OCP) is a bus-independent protocol that meets all the core-centric considerations discussed above and completely captures ALL of an IP core's communication requirements. The highly configurable OCP is not a one-size-fits-all protocol, but is instead analogous to a continuum of protocols that have a common definition structure. Sideband signals are explicitly supported via optional extensions to the basic OCP for reset, interrupts, errors, control/status information, etc. In addition, a generic flag bus is used to accommodate a core's unique signaling needs. The optional test interface extensions of the OCP support scan, JTAG and clock control, enabling debug and manufacturing test of the core when integrated into the System-on-Chip. A core's specific OCP configuration is therefore tailored to match the core's requirements exactly. A simple, low-performance core can have a very simple interface, while a complex, high-performance core can be accommodated just as effectively.

An IP developer can therefore complete an IP core design using the OCP interface. No end-application knowledge is required beyond the OCP, allowing complete independence between members of (often) global design teams. The system integrator is also free to choose the on-chip interconnect that best suits the system requirements of the application, then effectively "wraps" that interconnect to present OCP interfaces to the cores.

An IP core utilizing the OCP as its native interface can be easily reached by any bus structure the end-customer chooses through simple bridge or "wrapper" structures. Since the OCP doesn't constrain a core's functionality, every bus bridge to the OCP is able to reach that core's maximum capabilities. An IP developer could also pre-design a selection of bus bridges for some of the more common, non-OCP-compliant bus structures that a customer may choose. The work required to design such an OCP interface wrapper for a core is bound by the distinct choices that the OCP protocol itself offers, so there typically is only a regular set of wrappers that need to be provided. In fact, the wrapper generation process is regular enough to be amenable to automatic interface synthesis.

The alternative of designing multiple bus bridges from a core whose native interface was made to conform to a bus-centric protocol (one that may have been chosen by an IP designer who perceived that bus to be the most popular at the time of implementation) creates a starting point with rigidly defined limitations. Whenever there are differences in data and address presentation sequences between that core's rigid native bus protocol and the target bus, the core's performance will likely suffer. This is due to the bridge-on-bridge effect of having to correlate the signaling between the two disparate bus structures at their lowest common denominator. The implementation gate count for the bridged core is also likely to be higher.

An interesting and very relevant customer-based case study showed that installing the OCP on a slave USB core as the native interface, then building a bridge to one of the ARM AMBA bus protocols, required no more implementation gates than installing the AMBA AHB protocol as the core's native interface. In this instance, both implementations also passed through the full capabilities and performance of the core, although the AHB-native core required custom-defined implementations for all control and test signals, since the AMBA bus standard did not directly address their implementation. When these two cores were further interfaced to an IBM CoreConnect bus protocol (the OPB), the OCP-native core simply required a replacement bridge that again delivered all the core's capabilities and performance to the OPB. The AHB-native core, however, required incremental bridge logic from the AHB interface and was only capable of performing at half its bandwidth capability to the OPB due to the differences in address and data signaling between the two buses.

In summary, the core-centric OCP is an openly licensed, royalty-free protocol that does not impose restrictions or interfere with an IP core's inherent capabilities. It is scalable and configurable to match the different communication requirements associated with different IP cores. The OCP functions ideally as a native IP core interface since bridges to any bus or integration structure can be implemented without the gate count or performance penalties typical of bus-centric protocols. Cores with OCP interfaces and wrapped interconnect systems enable true plug-and-play hardware integration, thus allow-

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Socket Interface Tapped

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The c55x DSP core has to support an in-house bus interface in addition to OCP. After some investigation, it became clear that bridging from the dataflow segment of our OCP socket to this other interface was so simple that we could include the bridge in the interface design at no extra cost. This was an encouraging confirmation of our belief that it would be easy to bridge OCP to other interfaces.

As the design progressed, it became clear that using Open Core Protocol would actually save cycles compared with the original interface. This was in part because some of the constraints were removed from the OCP design, but did show that choosing OCP allowed designers to design interfaces which naturally fit into their blocks.

The adoption of OCP has made it significantly easier for us to use external IP in the core engine. Whereas before it would have been a challenge to integrate a memory controller from a third party and unthinkable to use one of the emerging interconnect generators, these options are now possible. One interesting possibility in this area is to make use of OCP's flexible burst protocol to reduce some of our FIFO requirements and improve performance by using a memory scheduler. ■

IP Core Interface Maximizes

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ing the system integrator to choose the best cores and best interconnect system for an application. Finally, verification and test suites, when written to the OCP, are completely portable to multiple designs, possibly requiring only minor and occasional adjustment for a particular interface bridge.

A standard IP core protocol is essential to the SoC design community, and OCP is the ONLY complete, fully supported and proven socket. With immediate adoption we are able to avoid the proliferation of non-compatible proprietary solutions and accelerate the market for, and reuse of, commercial and legacy IP cores. The complete, fully supported core-centric OCP delivers substantial and demonstrable benefits over older style bus-centric protocols.

OCP-IP members receive, at no charge, the CoreCreator™ tool as an OCP protocol compliance checker and environment "packager" for all the representations necessary for efficient reuse of an IP core.

The OCP specification is freely available for download at www.ocpip.org. ■

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