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OCP-IP News

Membership Announcements

OCP-IP is proud to announce the following new members:

Altera - is the pioneer of programmable logic solutions, enabling system and semiconductor companies to rapidly and cost effectively innovate, differentiate, and win in their markets.

Futurewei Technologies - a global provider of next-generation, fixed mobile convergence and end-to-end wireless technology improving capacity, efficiency and costs

Verification Technology Inc - supplier of acceleration, inclination, motion and pressure sensor solutions for automotive, medical, instrument and consumer applications.

WINLAB Rutgers University - an industry-university cooperative research center focused on wireless technology

King Faud University of Petroleum & Minerals - provides advanced training in the fields of science, engineering, and management; its goal is to promote leadership and service in the Kingdom's petroleum and mineral industries

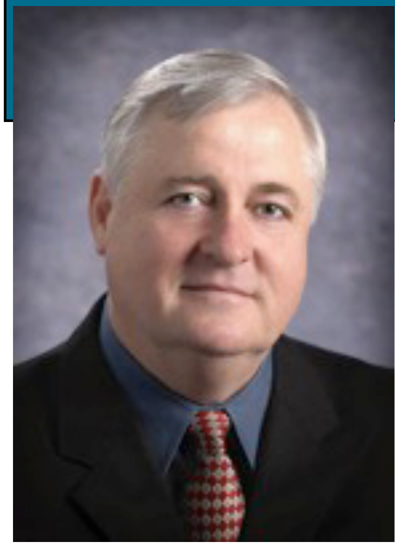
University Teknologi Malaysia - the largest Malaysian engineering-based university located at the southern tip of the Peninsular. It is renowned for being at the forefront of engineering and technological knowledge and expertise

Si2/OpenAccess Conference

October 14, 2009, at the TechMart in Santa Clara, CA.

The 14th Si2/OpenAccess+ conference will cover the increasingly inter-related areas of OpenAccess, Design for Manufacturability (DFM), and low power design. Updates on the industry adoption of OpenAccess will be presented along with plans for the future. Vendors in the OpenAccess and Low Power arenas will discuss their advanced capabilities and their experiences with low power formats. Exciting new developments in DFMwill be presented. Barry Dennington, NXP Senior Vice President and Chairman of the Si2 Board of Directors will provide the keynote address. There will be an evening session that will present demos of advances in the use of the technologies offered by Si2. This session will also serve as a valuable opportunity for networking. Refreshments will be served.

In recognition of the difficult economic times facing our industry, this Conference will be free of charge to all attendees. To register for the conference, visit http://www.si2.org/events_dir/register/oac10_2009.php



Ian Mackintosh
OCP-IP President and Chairman

President's Overview

The last few months have been extremely busy and exciting times for OCP-IP as OCP 3.0 has completed its member review and will soon enter general release. The next few months promise to be even busier as our Working Groups become tremendously active aligning their specifications and deliverables for the imminent arrival of OCP 3.0.

This edition of the newsletter has been specifically created to focus on a few of the new features that will become available in OCP 3.0. Our first technical article focuses on the new Cache Coherence feature of OCP, while our second technical article focuses on the new Power Management feature available. Stay tuned to future editions of the newsletter as we bring you in-depth technical features on other existing elements of OCP such as 2D Transactions and Non-Blocking flow control.

In other news we are pleased to announce that the OCP-IP NoC Benchmarking Working Group has entered an agreement with The Embedded Microprocessor Benchmarking Consortium (EEMBC), a non-profit corporation formed to standardize on real-world, embedded benchmark software to help designers select the right embedded processors for their systems. Through the collaboration EEMBC will provide benchmarks to the NoC BWG to facilitate their work creating multi-core traffic profiles for the industry.

OCP-IP has a robust, thriving, ever-expanding infrastructure designed to eliminate the need to internally design, develop, train and evolve a proprietary standard and accompanying support tools, freeing up critical resources for the real design work, saving hundreds of thousands of dollars every year for our members. As part of our ongoing efforts to ensure our members have the latest tools available, we are currently in discussions with two companies regarding tool donations for paying OCP-IP members; at least one of these will be available to members FREE, in the next quarter. These new tools will complement the CoreCreator II, and OCP conductor tools and SystemC TLM kits we already offer.

Finally, as always I would like to take a moment to thank each of our members who have given so graciously of their time and talent to write articles for this newsletter. Benefits of membership in OCP-IP include multiple marketing opportunities that we offer to our members (such as publication in this newsletter). Leveraging OCP-IP's marketing opportunities during these tough economic times is a great way to get the word out about products and services you offer directly to our focused OCP-IP community. For more information on the many opportunities available, email our marketing group at admin@ocpip.org.

Best Regards,

Ian R. Mackintosh

President and Chairman OCP-IP

Working Group Reports and Updates

Meta Data Working Group:
The Metadata Working Group (MDWG), continues to work on enhancements to fully capture OCP interfaces using the IP-XACT format defined by SPIRIT Consortium. The extensions describing OCP within existing IP-XACT format will be available to OCP-IP members in Q4 09. The MDWG is also working on OCP configuration checkers and interface compatibility checkers. Our MDWG includes representatives from Magillem, Nokia , Sonics, STMicroelectronics, Synopsys , Texas Instruments and Toshiba.

Debug Working Group:
The Debug WG focus for the remainder of 2009 will be on identifying required instrumentation signaling extensions and example cases for debug of multi-core systems that support OCP 3.0 cache and power management features. These may include SMP, AMP, multi-threaded, and other system architectures. Preliminary goals are for OCP 3.0 compatible debug systems white papers to be published in 1Q2010 with updated specifications to be developed later in 2010. The WG welcomes all contributions from OCP members for the OCP 3.0 debug system definition and development.

Specification Working Group:
The member review period for OCP 3.0 was recently closed and the Spec WG has reviewed and acted on all comments received. OCP 3.0 includes the additions of cache coherence extensions, power management signaling, a write response extension and a third consensus profile. OCP 3.0 will become the specification of record in 4Q09. Be sure to watch the OCP-IP website for further announcements about the release of the latest version of the spec.

NoC Benchmarking Working Group:
The NoC Benchmarking Working Group has recently entered into an agreement with EEMBC. The NoC BWG will use. EEMBC's MultiBench and related materials to create a set of traffic profiles that incorporate the data movements occurring in a multiprocessor system. In the future these Traffic Profiles will be available on OCP-IP's website and used for benchmarking Network-on-chip designs. This is an important step in standardization of NoC benchmarks as previously models of parallel application have not been available in the industry.

System Level Design Working Group:
The SLD's project to evolve and enhance the entire Transaction Level Modeling kit and support modeling is now complete, OSCI 2.0 compatible, and is available FREE from our website. The group is now focused on further advancing the TLM Kits to include support for the new features proposed in OCP 3.0. The next phase of the kit advancement includes collaboration with a strategic partner focused on software needs for semiconductors.

Marketing Working Group:
The Marketing Working Group has recently completed presentations at the EE Times System-on-chip Virtual Conference (link here) and the Software Defined Radio Forum. In addition we remain very active helping member companies compose and place their OCP-related articles and conference papers, while publishing the OCP-IP newsletter and our regular press releases. If your company would like assistance placing an article, prominently targeted to the industry or directly to our OCP-IP focused community, please contact admin@ocpip.org.

Using OCP and Coherence Extensions to Support System-Level Cache Coherence

By Chien-Chun (Joe) Chou, Sonics, Inc.; Konstantinos Aisopos, EE Dept., Princeton University; David Lau, MIPS Technologies; Yasuhiko Kurosawa, Toshiba Corporation; and D. N. (Jay) Jayasimha, Sonics, Inc.

Open Core Protocol (OCP) [1][2] is a common standard for Intellectual Property (IP)core interfaces. OCP facilitates IP core plug-and-play and simplifies reuse by decoupling the cores from the on-chip interconnection network and from one another. The OCP interface allows IP core developers to focus on core design without knowing details about the System-on-Chip (SoC) in which the core might eventually be deployed. Recently, numerous academic publications pointed out the benefits of hardware coherence in MultiProcessor SoCs (MPSoCs) [3][4][5], citing reasons such as enhanced performance versus software approaches, faster time-to- market, flexibility, and ease of programming.

Enabling hardware cache coherence support at OCP cores requires the OCP interface to generate and receive additional coherence messages in order to invalidate cache lines cached at the core side or transfer cache lines and their ownerships between OCP cores. In addition, the protocol extension needs to be flexible enough to support different system-level coherence schemes, such as any invalidate-based snoopy coherence scheme, or any directory-based coherence scheme. Other possible challenges in the design of a cache coherent heterogeneous system include dealing with different sets of cache line states across initiator cores, different protocols, and allowing multiple cache-line sizes.

In the following sections, the concept of OCP coherence extensions is described. Moreover, an example OCP-based coherence design utilizing the proposed OCP coherence extensions to support system-level cache coherence is also demonstrated.

Proposed Coherence Extensions to OCP

OCP enforces a point-to-point communication interface between two entities acting as the master and the slave of the OCP instance. Different types of communications can occur between the master and the slave of an OCP instance.

OCP Transfer and Transaction

An OCP dataflow communication (e.g., an OCP transfer) usually starts when the master presents a read request or a write request with data to the slave. The communication usually ends when the slave responds to the request presented to it, either by returning data to the master or by accepting the data sent from the master. One OCP data word is exchanged between the master and the slave in the above OCP transfer, where the memory location of the data word is given by the master. An OCP burst transaction can include a set of transfers similar to the one mentioned, so that multiple data words can be communicated between the master and the slave.

Example Cache Coherence Transaction

The need for separate coherence transactions and additional ports on OCP is best illustrated through an example. Since a memory cache line usually has a size of multiple OCP data words, it can be delivered between the master and the slave of an OCP instance by an OCP burst given the critical word's address, using a WRAP or XOR burst sequence. However, in a

Continued next page

multiprocessor system where cache coherency among multiprocessor caches is maintained by hardware, the agent involved in a cache coherence transaction happening in the system can include the home of the cache line (e.g., memory), the latest owner (e.g., a processor core) of the cache line, many possible copy holders (e.g., many processor cores) of the cache line, and the processor core attempting to obtain the latest copy of the cache line into a specific state. It is clear, but important to notice that all communication patterns needed for completing the cache coherence transaction described are not covered by only treating each processor core as an initiator OCP core and utilizing the request and response dataflow between the master and the slave, only.

For instance, an initiator processor core should be able to start a cache coherence transaction, to accept and answer to a cache line inquiry resulting from a cache coherence transaction, and to possibly return its latest cache line copy to the transaction's originator. In other words, each processor core needs to (1) send coherent commands using the existing OCP interface (i.e., the master port1); (2) have an additional OCP slave port in order to receive cache inquiries and invalidations; (3) have a new OCP coherent state signal for answering cache inquiries; and (4) have a new OCP response to indicate the carrying of a coherent state without transferring cache line data words. Other capabilities can also be essential for each coherence transaction, such as: the identification scheme (for routing) used among OCP inquiry/invalidation ports mentioned above, and the distinction between a "self" cache line inquiry/invalidation and an inquiry coming from others, e.g., a "system" cache line inquiry/invalidation.

OCP Coherence Extensions

In order to support system-level cache coherence, such as in a directory-based MPSoC, the OCP 2.2 port needs to be extended with new coherent signals and signal encodings to deliver coherent transactions. From the system design point-of-view, each processor core with its caches and the directory module are now considered as a coherent initiator and a coherent target, respectively. In addition, a new OCP port, the OCP intervention port, is introduced and attached to each coherent initiator or target to allow coherent cores to probe and update each other coherent cores' cache coherency states, as well as to transfer cache lines. *Figure 1* shows a possible block diagram of a directory-based multiprocessor on-chip design using OCP and coherence extensions. The figure further illustrates roles played by the processor cores, the directory module, the memory sub system, and the I/O device – that is as coherent initiators, as coherent target and OCP initiator, as OCP target, and as OCP target, respectively. Note that each coherent initiator (e.g., a processor core) has an outgoing OCP coherence extensions (OCPce) port and an incoming OCP intervention (OCPi) port. On the other hand, a coherent target (e.g., a directory module) has an incoming OCPce port and an outgoing OCPi port.

To read the complete article, click here.

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Adding support for power management in OCP
The OCP Disconnect Protocol

By Christophe Vatinel, Texas Instruments

According to Moore's law, System-on-Chips are continually becoming more complex and integrating more components, enabled by the continuing size reduction of silicon technologies. On the other hand, power consumption does not follow the same reduction ratio because of increasing leakage in deep sub-micron technologies. Hence, new power management techniques are being progressively deployed within the SoC in order to reduce power dissipation as much as possible.

This paper exposes some of the new architectural problems that exist in today's complex SoCs involving power management techniques. The concept of interface disconnection is introduced as a viable solution and the OCP disconnect protocol is detailed as an implementation of this concept. Finally, several usage examples in a power management framework are provided.

Emerging problems

A typical SoC can be partitioned into several domains that can be managed more-or-less independently, with respect to power management. Several power management techniques may be used: such as reducing clock frequency, lowering voltage, gating the clock, switching to retention mode, or switching off. This list is not exhaustive and detailing all power management techniques is not the purpose of this paper. However, one must realize that with some of these techniques, the affected components are not

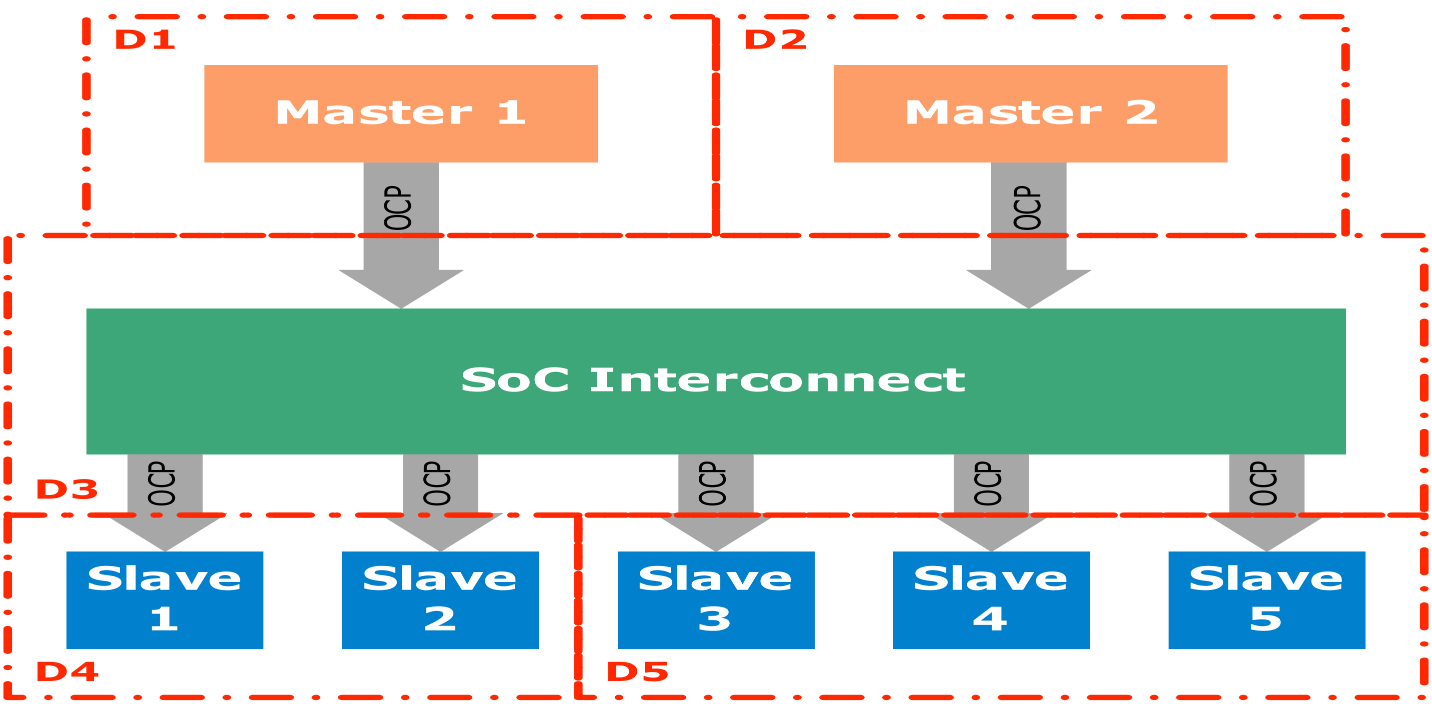

Figure 1: SoC architecture example

responsive to any input. At most, signals from a component in such a state can be forced to a pre-defined value thanks to a clamp technique. Such states will be referred to as "sleep" states in the rest of this article.

On the other hand, the Open Core Protocol defines a point-to-point, fully synchronous interface protocol that can be used as an internal communication method. Figure 1 shows an example of a simple SoC with several power domains, using an OCP protocol for interconnection.

Putting a slave domain to sleep:

A "slave domain" has at least one OCP slave interface at its domain boundary (e.g. D3, D4, D5). Before putting a slave domain to sleep, one must ensure that any OCP interface from another domain, connected to one of the slave ports of the domain, is in a state where all OCP transactions are completed (i.e. there are no outstanding transactions). Not doing so can result in various SoC malfunctions.

If a slave domain is being put to sleep while another domain is sending transactions to it, then the corresponding master (possibly the interconnect) will likely become stuck on its OCP master port. If a slave domain is asleep and some transactions to it are not completed, then the corresponding master will also become stuck due to lack of response. In both cases, there is no easy way to recover from such a situation. Also note that these malfunctions may propagate upstream from the interconnect toward the master initiating the transactions, ultimately resulting in a major failure.

Putting a master domain to sleep:

A master domain is a domain having at least one OCP master interface at its domain boundary (e.g. D1, D2, D3). Before putting a master domain to sleep, one must ensure that any OCP interface to another domain, connected from one of the master ports of the domain, is in a state where all OCP transactions are completed (i.e. there are no outstanding transactions). Not doing so can again result in various SoC malfunctions.

If a master domain is being put to sleep while sending a transaction, then the corresponding slave (possibly the interconnect) will likely become stuck or even corrupted. If a master domain is asleep and some transactions are not completed, then the corresponding slave will also likely become stuck. In both cases, as is the case for slave domains, there is no easy way to recover from such a situation. Also note that these malfunctions may propagate downstream from the interconnect toward the slave target of the transactions, again resulting in a major failure.

It might be thought that software could be relied upon to guarantee the necessary condition is true before performing a sleep transition. However, in complex SoCs with multiple masters and a complex interconnect, it would be very difficult for software to monitor transaction completeness. Also, it is possible that some masters are totally independent of software. A debug master IP is in this category.

For the rest of the article click here.

About the author:

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STEP - Automated Synthesis of On-Chip-Bus Protocol Transducers

Masahiro Fujita
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VLSI Design and Education Center (VDEC) in the University of Tokyo has created a new tool called STEP which stands for SynThesizing Environment for Protocol transducer. The tool automatically generates RTL description of transducers between two on-chip protocols. STEP can generate minimum latency protocol transducers from the automaton based protocol definitions and is capable of handling complicated on-chip interfaces including non blocking, burst mode, out-of-order, and others. Evaluation results show that it takes only a few minutes to generate protocol transducers for the full set of OCP.

Incompatibility of Communication Protocols in Modern SoC Design
With increasing complexity of the circuits on a single chip, IP-based design methodology is attracting attention to shorten the design cycles. By re-using existing designs within new designs, the design period is expected to be significantly shortened. In IP-based designs, one of the most important issues is the connectivity between IPs. Since IPs usually have their own interfaces, they cannot communicate with one another if they use different protocols. In other words, IPs which can normally communicate directly to another IP may be limited if there is an interface mismatch.

In actual designs, designers usually insert protocol transducers (also called wrappers or bridges) between IPs with incompatible protocols, which consume additional development time. As a result, the advantage of IP-based design is reduced. To resolve the problem, automatic synthesis of protocol transducers is an attractive solution. It, however, is not at all straightforward, as the state-of-the-art protocols such as OCP have various complicated functionalities such as non-blocking (pipelined) and out-of-order transactions. Unfortunately, the synthesis methods proposed so far to date, often have trouble accommodating such advanced features in complex protocols, because the synthesis algorithms used in the previous methods cannot support these features. VDEC has developed an automatic transducer synthesis tool, STEP, which is capable of handling protocols with such advanced features as mentioned above.

To read this entire article, click here.

Recent Publications

Available in the OCP-IP Press Room at www.ocpip.org/pressroom.

Press Releases

June 3 - OCP-IP Announces Availability of New Network on Chip Benchmarking White Paper

Articles

September 15 -OCP-IP SOLV eases SoC verification
EDA DesignLineChip Design Magazine

August 11 -IP Interface Standards
ICJournal

August 07 - Application modelling and hardware description for network-on-chip benchmarking
IET Digital Library

June 22 Viewpoint:Capture OCP systems in IP-XACT 1.4
EDA DesignLine

June 18 - EDA Remains The Enabler of Much-Needed Innovation
Electronic Design

Announcements: Now Available

OCP Checker Now Part of CoreCreator II

The OCP checker a fourth-generation solution for validating protocol compliance of master and slave devices using OCP. It is based on SystemVerilog assertions (SVA) and can be used with all major logic simulators. It supports the complete set of protocol compliance checks defined in the OCP specification and spans the full range of OCP socket configuration options. The OCP checker can also generate trace files in the standard ".ocp" format for post-processing. The checker can be obtained, as part of CoreCreator II here.

OCP 2.2 Specification Rev 1.1

The Specification Working Group officially released the OCP 2.2 Specification Rev 1.1 in May 2008. This version incorporates published errata and two consensus profiles from key OCP-IP members, and adds a trace file format (.ocp) description. OCP 2.2. Revision 1.1 is now available on the OCP-IP Web site. For a copy complete our Research License Agreement.

Debug Specification Version 1.0

The Debug Specification provides guidelines and recommended signal interfaces for on-chip debug of OCP-based systems and related multicore architectures. It provides a framework for IP and tools providers to develop comprehensive and re-usable debug and instrumentation environments that provide on-chip analysis and control features. These include trace, triggering, multicore synchronization, etc., along with recommendations for integration within ESL environments. The specification can be downloaded here.

Network-on-Chip Benchmarking Specification, Part 2

Part 2 of the two-part NoC Benchmarking Specification presents a generic NoC architecture, a comprehensive set of synthetic workloads as micro-benchmarks, workload scenarios and evaluation criteria. These micro-benchmarks enable you to measure and pinpoint particular properties of NoC architectures, complementing application benchmarks. For more information, click here.

Network-on-Chip Benchmarking Specification, Part 1

The specification presents a modeling methodology for applications running on multicore systems and it defines an XML format for documenting and distributing NoC benchmarks. It defines a black-box view of the processing elements that discloses only the relevant computational aspects for interacting with the on-chip data transport mechanism. Download our NoC white paper for more information

Transaction Analysis Tool

The Tool is an innovative, detailed OCP transaction viewer that enables fine-grained analysis of bus transactions. A complete transaction sequence can be traced from request to response along with a host of related information about the transaction. For a FREE copy contact admin@ocpip.org

OCP SystemC TLM Kits

The new kit is the first, and most advanced TLM-2.0 based, industry-ready kit in existence today. The kits significantly increase performance, ease of use and ensures alignment with the OSCI 2.0 standard. The kits are free as part of OCP-IP membership. For more information contact admin@ocpip.org