



## IP - European Style

IP07 was the tenth meeting in Grenoble of IP providers and users under the umbrella of Design and Reuse ([www.designandreuse.com](http://www.designandreuse.com)), the IP portal. Europe editor Dick Selwood compares facts and marketing-speak.

It sounds like the start of a joke. "There were three processor manufacturers at a conference..." And when the three processor manufacturers were asked, "What is needed to service the power-conscious emerging mobile video marketplace?" they came up with three similar answers. The man from MIPS said that it would be serviced by the ecosystem that has developed around a MIPS architecture with added analog capability from Chipidea, their recent acquisition. The man from ARC said that the true path forward was a reconfigurable, heterogeneous multiprocessor architecture, and there was a family of ARC video sub-systems to prove it. And the man from SiliconHive said that the true way is a coupled massively-parallel architecture with a parallelising compiler, and here is the starting point, the VSP2000 family. The chairman of the panel session was from Cadence, and he said that, whatever the solution, it would need EDA tools that were

power-aware.

In fact there was more commonality than a joke might suggest. They all agreed that the power requirements of mobile video – and mobile video was chosen as currently the most processor-intensive and therefore the most power-demanding mobile application - were going to be solved only by a holistic approach, starting with an analysis of the functionality of the device, what it would be doing, and what bits would need to work with other bits for specific tasks. From this it should be possible to build an architectural model to explore different trade-offs and undertake power analysis. The end product could then be designed so that applications would run only those sections that are needed, powering down the rest. True, different trade offs, such as process technologies, clock gating, and software designed for lower power would also help, but the key has to be to look at the high level of the system.

This session was typical of many at IP07, a mixture of good common sense and industry insight blended with marketing-speak. In most sessions, the marketing quotient (or BS factor) was usually below five on a one to ten scale, which left plenty of space for good information -- although there were some panel presenters who seemed unable to turn off the jargon generator or to disable the "get the company name or a product mention in at least every three sentences" routine.

Jim Tully of Gartner sees the IP business as still set for significant growth. Two trends will fuel the growth – standards-based IP and the exploding consumer market. Waves of new standards - for buses, for memory interfacing, and for communications, to name just three - mean that the implementers will find it easier to use IP than to learn the details of a new standard or, even worse, an emerging standard. (This ties in with the prediction that re-configurable IP will also show significant growth, particularly to cope with emerging standards.) The consumption of semiconductors by the consumer electronics industry has grown from 25% of all semiconductors produced in 1995 to 55% in 2005, and growth is predicted to rise to 62% in 2015. But there are risks in the consumer market: Procter and Gamble, acknowledged experts in marketing to the consumer, fail with 75% of their new product launches -- but when a product is a winner, it wins big-time.

The idea that standards will provide the winning horses in the IP stakes was echoed by a number of speakers, including EDA giant Synopsys. Other speakers welcomed standards-based IP, particularly if it includes a bundle of software and stacks as well as silicon layout.

Standardization for IP (rather than IP for standards) was a topic in its own right, both in panel sessions and in conversation, particularly with the recent closure of the VSIA and the transfer of its property to IEEE. Other standards bodies still exist, and the alphabet soup doesn't help too much – SPIRIT and OCP-IP are still doing a lot of work to make it easier to integrate separate blocks of IP in a single device. (Infineon has its own internal standards for IP generated in-house.) However, there is no single co-ordinating body for IP standards, and this may be an obstacle in their wider use.

An interesting paper was that by Ron Collett of Numetrics. The starting point is the melancholy fact that most SoC design projects overrun, some very significantly, and yet IP and reuse was meant to reduce the effort required to create a device. He produced a graph based on an analysis of over 1200 completed designs by the leading IDMs that showed that reusing by adding IP started to have a significant impact on the project life only when the majority

of the design was straight reuse, which is rarely the case. The most startling illustration was the issue of a straight re-implementation of a device with “only” a 10% change. If the 10% is a single module, then the project should be concluded relatively quickly. But if the 10% is on each module of the design, then it could take a significant amount of effort (and time) to complete the project -- time that will probably be under-budgeted.

In many panel sessions, there seemed to be similar concerns – quality of IP, difficulty of integration, and verification issues. An area that was a significant concern ten years ago was security – making sure that the IP was not hi-jacked - and a lot of time was devoted to watermarking, obfuscation and encoding. This died down as vendors and users learned to trust each other in good faith (on the whole). There was a startling (to a European’s sensibilities) presentation on patent support, where the message seemed to be “SUE the b.....s. Sue them early and sue them hard, and build up your own patent portfolio so that you have lots of grounds on which you can sue.” OK, this is an exaggeration, but it was pretty much the approach that was put forward.

Returning to quality: many large companies have implemented special programmes to verify IP quality, but smaller companies are going to have to buy from companies that they trust. And integration into designs and verification of the device will continue to offer challenges. (Back to the need for standards.)

While talking of smaller companies, it was only once that I heard FPGA mentioned. And that was in a question in a technical session, where the questioner wanted to know about the speaker’s support for FPGAs. Given the massive growth in the use of programmable logic and in the capacity of the devices, it does seem strange that there was neither an FPGA thread at the conference nor a panel session among the keynotes.

An area that did make an appearance was analog and mixed-signal IP. Just as with emergent standards, analog is difficult, and experts are rare. Even integrating analog/mixed signal into a digital design has challenges, particularly for an engineer with limited experience outside the digital domain. Here again, users want a total package that can be dropped in, but the package has to include accurate SPICE models to make development and debugging less complex.

Design and Reuse, the organiser of the conference, is a web-based portal that provides a link between IP suppliers and IP users. Gabrielle Saucier, the founder

of Design and Reuse, used the statistics of the site to provide a quick view of the IP community. The site has 32,000 registered users and 200,000 page views a month, with most users coming from Asia (42%). The US has 30% and Europe 25%. They hold details of nearly 6,600 separate IP elements from 400 providers. The provider breakdown is interesting, with EDA vendors, design centres, fabless IC vendors, and foundries providing the overwhelming majority of the material, presumably to drive the usage of their tools or services.

But IP07 was also a birthday party, and, being in France, a birthday means a feast. There was a magnificent conference dinner with wines and accompanying food, chosen to provide a virtual tour of the French regions. There were also, like in all good birthday parties, prizes. Awarded for the best papers in the technical conference, they were sponsored by CEA/LETI, the French national electronics research centre. The prize for Design Methodology was awarded to "Virtual Prototyping Environment for Multi-core SoC Hardware and Software Development" by Syed Saif Abrar and Aravinda Thimmapuram of NXP Semiconductors, Bangalore, INDIA. That for IP Design went to "A 0.79-mm<sup>2</sup> 29-mW Real-Time Face Detection IP Core" by Yuichi Hori, Yuya Hanai and Tadahiro Kuroda of Keio University, Yokohama, Japan, and this year a special prize was awarded to "Generic Driver Model using Hardware Abstraction and Standard APIs" by Amar Amar, Shirish Joshi and Don Wallwork from Cisco Systems Inc. (These papers and many others are available on the web at [www.design-reuse.com](http://www.design-reuse.com))

IP is much more than just processors (although ARM was strongly present), and, despite the decline in ASIC starts, it is a strong business and continuing to grow. The next ten years will be interesting.

by Dick Selwood, Embedded Technology Journal

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