Volume 6 Issue 2
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OCP-IP News

The Official Newsletter of the Open Core Protocol International Partnership

Membership Announcements

OCP-IP is proud to announce the following new members:

Axell Corporation – Develops and sells original LSI of graphics and sound used for embedded systems. Axell is conducting research and development into an original compression technology, and has subsequently enhanced the value of their products.

Beceem Communications – The leading provider of high performance chipset solutions for the Mobile WiMAX market, and was the first to introduce terminal chipsets for the Wave 1 and Wave 2 WiMAX Forum profiles, which are based on the IEEE 802.16e-2005 Mobile WiMAX standard.

Digimarc – Digimarc's digital watermarking technology provides a persistent digital identity for various media content and is used to enhance the security of financial documents, identity documents and digital images, and support other media rights management applications.

Embedded Systems Laboratory – National Sun Yat-Sen University (Taiwan) –The Embedded Systems Laboratory addresses the design, integration, verification and use of hardware and software in embedded systems. Their focuses may include (but are not limited to) high performance/low power/low cost processor design and optimization, SoC design for networking/security/multimedia, IP design, real-time operating systems, testing/debugging, system integration, and the related software/firmware techniques.

Verilab – An elite international team of verification experts who specialize in solving the toughest problems in VLSI functional verification, from chip rescue and critical path pruning, through sophisticated verification IP development, to complete methodology re-engineering.

Industry Events

Multicore Expo

April 1 – 3, 2008
Santa Clara
Convention Center
Santa Clara, California

OCP Technology Forum 2008

May 29, 2008
Shinyokohama
Kokusai Hotel
Yokohama, Japan

Design Automation Conference 2008

June 9 – 13, 2008
Anaheim Convention
Center
Anaheim, California

For more details on OCP-IP events and presentations, please visit www.ocpip.org/pressroom/schedule/tradeshows.

OCP-IP Mission Statement:

Promote and support OCP as the complete socket standard that ensures rapid creation and integration of interoperable IP cores.

President's Overview

By Ian Mackintosh
OCP-IP Chairman
and President

Throughout the past quarter, OCP-IP has continued its commitment to leadership and an ongoing expansion of its global presence by sponsoring several industry events, including EDAC's annual CEO Forecast and ECSI's System Debug Workshop, which was held in conjunction with DATE '08. OCP-IP will be sponsoring this same System Debug Workshop at DAC, as well as the second annual OCP Technology Forum in Yokohama, Japan, scheduled for May 29, 2008. Be sure to check the OCP-IP Web site for more event details as they become available.

Every year around DATE, OCP-IP allows members to post product presentations highlighting their use and support of OCP on our Web site. For the past several years these presentations have been, and continue to be, one of the most highly visited areas of the site. This year's round of presentations are contributed by companies including AerieLogic, Cadence, CoWare, Jeda Technologies, Mercury Computing Systems, Synopsys, Yogitech, and VaST Systems, as well as from the OCP-IP Debug and Network-on-Chip Benchmarking Working Groups. We are pleased to announce that the 2008 OCP-IP DATE partner presentations are now available free, at www.ocpip.org/pressroom/schedule/speaking/papers_presentations/.

On the technical front, the OCP-IP Debug Specification has completed Member Review and was formally announced at ECSI's System Debug Workshop. The specification details an approach to a standardized OCP-bus compliant debug interface. The solution, an optional OCP port, implements a debug interface socket that can be added to all cores and IP blocks. To download your copy of this specification, please see www.ocpip.org/socket/ocpspec/.

The OCP-IP Governing Steering Committee (GSC) has recently approved the formation of a working group focused in the area of Metadata. The aim of this working group ("MDWG") is to enhance Metadata schemes to ensure they accurately and effectively represent and capture all of the valuable information available from the OCP interface. If you would like to participate in this, or any, of OCP-IP's Working Groups, we invite you to immediately contact admin@ocpip.org.

The work of OCP-IP's System Level Design Working Group in the area of TLMs and standardization was featured in a recent story on Virtual Prototyping by CMP's Rick Merrit (www.ocpip.org/pressroom/articles/Recently_Published_Articles/). Lastly, I recently had the pleasure of participating in a roundtable discussion on the issue of design standards. The discussion was hosted by Peggy Aycinena of EDA Weekly and featured representation from various companies and standards bodies including: IEEE, SPIRIT, Mentor, and IP Extreme. Based on this recent discussion, I am pleased to say that there appears to be a growing consensus and optimism about EDA standards, which is good news for everyone involved in the industry!

Regards,

Ian R. Mackintosh
Chairman and President, OCP-IP

Working Groups: Reports and Updates

Debug Working Group

The OCP-IP Debug Working Group recently published their OCP Debug Specification, which provides a set of guidelines and recommended signal interfaces for on-chip debug of OCP-based systems and related multicore architectures. The group is now focused on specifying a supporting analysis infrastructure, including API, tools, and reference designs for multicore and ESL integration. Members interested in contributing to either the reference designs or the specification itself should contact admin@ocpip.org. The OCP Debug Specification is available on the OCP-IP Web site.

Functional Verification Working Group

The Functional Verification WG continues to evolve a proposal for evaluating performance at an individual OCP port with the intention of adding this to the Verification section of a future version of the OCP Specification. The Functional Verification WG is also reviewing the existing Verification sections for inconsistencies.

Marketing Working Group

The OCP-IP MWG has recently distributed important press releases announcing the Network-on-Chip and Debug Specifications, as well as the availability of CoreCreator II. The MWG is now busy preparing for exhibitions at Multicore Expo, the second annual OCP Technology Forum in Yokohama, Japan, and the Design Automation Conference. If you are an OCP-IP member and would like to be contacted about participation in future events, please send an email to admin@ocpip.org.

Metadata Working Group

The MDWG is a newly formalized activity inside OCP-IP to capture OCP interfaces using the IP-XACT format defined by the Spirit Consortium. The first step for the MDWG is to develop a plan to describe OCP with the existing IP-XACT XML format. If some of the OCP characteristics cannot be described with the current IP-XACT, the MDWG will develop its own extensions to the format and work with Spirit member companies to incorporate these extensions into future releases of IP-XACT. The MDWG has existed since the beginning of 2008 and includes representatives from Nokia, Sonics, STMicroelectronics, Synopsys, and Texas Instruments.

Network-on-Chip Benchmarking Working Group

The NoC BWG recently announced the completion of member review for Part 1 of the NoC Benchmarking Specification. Part 1 details requirements and features for application programs, synthetic micro-benchmarks, and abstract benchmark applications. It also discusses ways to measure and benchmark reliability, fault tolerance, and testability of the on-chip communication fabric. Part 2 of the NoC Benchmarking Specification is scheduled to be released later in the year. Members interested in participating in the NoC BWG should contact admin@ocpip.org.

Specification Working Group

The Specification Working Group continues to work toward the release of OCP 3.0, which will consist of cache coherence extensions, power management signaling, and a third consensus profile, among other tentative inclusions. The first two consensus profiles from key OCP-IP members will be released in a specification revision prior to 3.0.

System Level Design Working Group

The System Level Design WG recently released the OCP Transaction Level Monitor Channel version 2.2.1. This release is available on the OCP-IP Web site to OCP-IP members and the general public. The SLD WG is in the beginning stages of upgrading the entire kit to reflect a style of modeling being proposed by OSCI. This redevelopment will ensure the OCP-IP kit remains simple, fast, and easy to maintain as a leading-edge offering, even into CY09.

Technical Vision Working Group

The TVWG held its annual strategic planning session for the organization in February 2008. This resulted in all OCP-IP working groups confirming their specific roadmaps and goals for work to be completed in 2008. The OCP-IP Governing Steering Committee will continue to monitor and support these targets throughout the year. ■

Single Flow for Interconnecting OCP-based IP and Auto-generating Design Views

Jo Anderson and Mike Smith
Beach Solutions

The latest challenge facing SoC teams is the construction of a design flow that seamlessly combines:

- A complex central Interconnect Matrix
- Auto generation of a diverse range of system design views

While suppliers of Interconnect Matrix components provide complex architectures for hardware, the SoC team is also responsible for producing other associated design view outputs such as documentation and code for software development, test and verification.

Ultimately this team is responsible for delivering a fully tested, documented and usable product – on time.

In this article, we outline a flow, based around Beach Solutions® software, which results in seamless interoperability between disparate tools and methods.

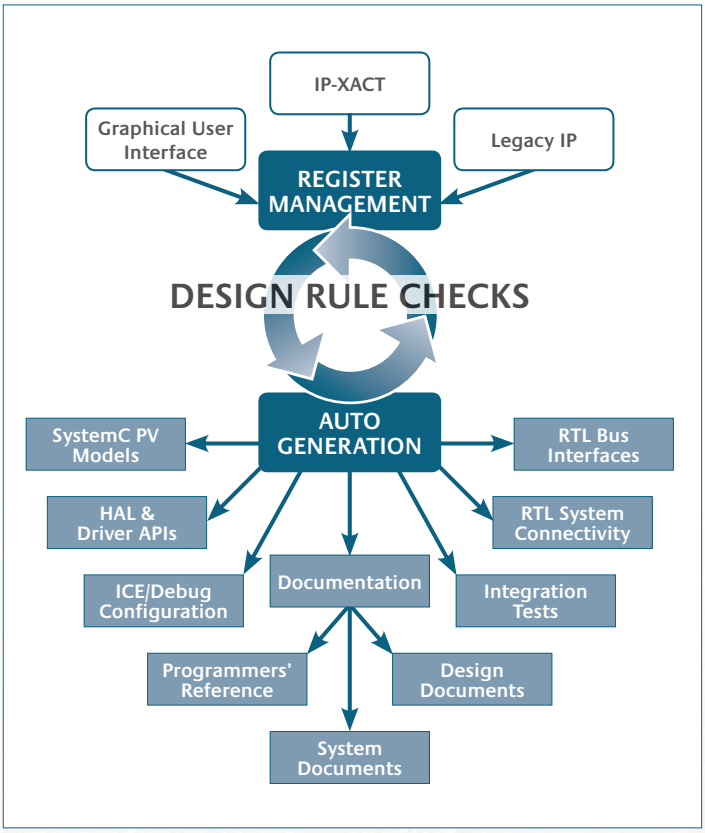
Central Interconnect Matrix

A central Interconnect Matrix allows a designer to create multiple memory maps and control communications paths based on specific master and slave combinations, easily and quickly.

The design and creation of an Interconnect Matrix component is well defined and tools providing suitable architectures are available from companies such as Sonics.

Auto design view generation

SoC design teams now realize the benefits of storing register address map information in a central repository and use auto-generation techniques to create a diverse range of design views for software developers, hardware designers, verification engineers and documentation teams. Initiatives such as SPIRIT (IP-XACT) and software companies like Beach Solutions provide out-of-the-box solutions for the capture of IP and system interface information (in a generic form) and the auto-generation of design views. The breadth of designs views that can be generated depends upon the depth of information that is captured and stored.



Beach Solutions advocate that, in addition to other attributes, there are 3 essential elements to capturing interface information for maximum auto-generation purposes:

1. Physical interfaces: discrete ports, point-to-point signals and connections
2. Physical memory map: register, bitfield and memory definitions
3. Transaction level: base addresses for located IP and allowable initiator/slave communications

The Beach Solutions generic flow is based on a three-step methodology: capture, validate and auto-generate a broad range of design views.

Interconnect Matrix – more than a black box

The architecture of an Interconnect Matrix is typically hidden from the SoC designer – indeed this is one of its advantages. Unfortunately, this means that for auto-generation purposes an Interconnect Matrix is

typically captured as an IP-core with just physical interface information, i.e. only one of the essential elements.

This means that you effectively have a black box IP core in your system, to which other cores are physically connected, from which you need to auto-generate a complete set of system views.

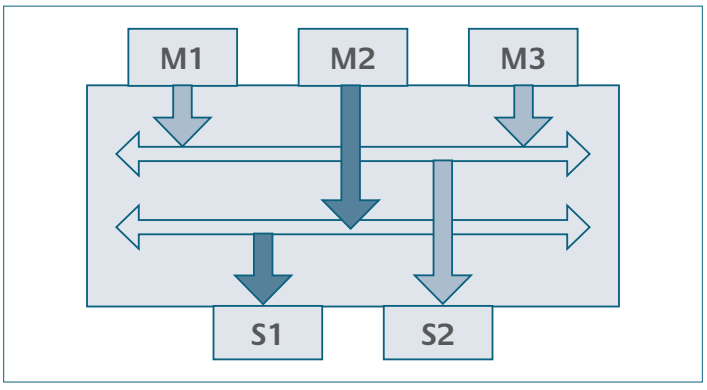
The physical interface information permits auto-generation of some hardware outputs (such as RTL representation of system connectivity), but precludes most software and verification views.

The success of a design flow incorporating auto generation tools depends upon capturing the minimum amount of information that will permit generation of the maximum number of different design views. So, the solution to incorporating an Interconnect Matrix component into such a flow is to treat it as a 'grey' rather than a black box.

Interconnect Matrix – a grey box...

For a scalable and generic solution, the Interconnect Matrix component should be viewed as grey box. This means that when one or more such components are instanced in a system, visibility of the transaction-level communication paths through them is known.

Using Beach Solutions EASI Tools as an example, an Interconnect Matrix is captured as an EASI database 'System' object (similar to IP-XACT component). For example, an interconnect that allows Master M1 and M3 to access S2 but Master M2 can only access S1. See figure below:



IP core representation

Other IP cores are captured as EASI database 'IP Block' objects, each having a corresponding transaction interface(s) to the Interconnect Matrix component. Information about memory mapped registers, bitfields and memories is captured within each IP Block.

System representation

The System object in the EASI database is also used to represent the top-level of the final system. Each system can contain:

- Instantiations of components
- Transaction-level communication paths
- Point-to-point connections

Maintaining these levels of information in the captured data means that the 3 essential requirements for maximum auto-generation have been met and hence generation of a broad range of design views becomes possible.

Proposed design flow

The proposed iterative design flow that allows for auto-generation of multiple design views for a system with a complex OCP Interconnect Matrix uses tools readily available from commercial tool vendors.

1. Auto create Interconnect block

Use a graphical wizard and sophisticated GUI, available in EASI Tools, to capture the Interconnect Matrix component as a system with physical ports, parameters and transaction level communication paths. The wizard can be pre-configured with master and slave interface types (for example OCP) together with any associated interface constraints (parameters). ■

For the complete article, please visit
www.ocpip.org/pressroom/articles/Recently_Published_Articles.

Events

DATE 2008

DATE 2008 was a tremendous success for OCP-IP! In addition to the presence of our popular exhibition booth, OCP-IP sponsored ECSI's System Debug Workshop, held in conjunction with DATE, where the formal announcement on the availability of the OCP-IP Debug Specification was made. Aside from this important industry announcement, the System Debug Workshop held sessions which addressed debug challenges and industry requirements and provided attendees with an opportunity to watch debug tool presentations and demonstrations. For the third year in a row, OCP-IP also solicited our always-popular, OCP-related DATE partner presentations from member companies, which are available free on the OCP-IP Web site (www.ocpip.org/pressroom/schedule/speaking/papers_presentations/). ■

Multicore Expo

OCP-IP is a proud sponsor and participant of the Multicore Expo. Please register (www.multicore-expo.com) to attend and you can join Bob Uvacek, VP of Engineering at Botana Inc. and Chairman of the OCP-IP Debug Working Group for the following panel discussion:

Debugging Multicore Software - Hope for the Bewildered Programmer

Moderated by Jim Holt, Manager: Advanced Core Architecture Enablement, Freescale.

Also, be sure to stop by our booth during the exhibition hours:

Tuesday, April 1 - Exhibit Hours:

12:10-14:00 (including lunch)

17:40-20:00 (including reception)

Wednesday, April 2 - Exhibit Hours:

12:30-14:00 (including lunch) ■

University Corner

Test Wrapper Design for OCP Cores

Cristian Grecu, Yongsoon Lee,
Andre Ivanov
University of British Columbia

Researchers at UBC are working to define an improved test wrapper for network-on-chip systems that use OCP-compatible functional cores. Traditionally, a combination of test wrappers and test access mechanisms are used to transport and apply test vectors to the individual cores of systems-on-chip. There are two options to combine a test wrapper with the OCP-compatible core under test.

First, the OCP core can be simply wrapped with a standard test wrapper such as IEEE 1500, and then connected to a dedicated test access mechanism (TAM) that delivers the test data when the chip is in the test mode. This method has the advantage of simplicity, but requires additional global interconnects (the test access mechanism).

A second option that the UBC team is investigating is to insert the test wrapper in between the IP core and its OCP interface. This makes possible the use of the functional interconnect and protocols (on-chip network and OCP core interface) to deliver test data to the functional cores, without a need for additional test protocols and test access mechanisms. A distinct benefit of this approach is the ability to speed-up the test procedure, taking advantage of the larger bandwidth of the functional interconnects. Another advantage is the ease of integration with CAD tools available for OCP-based design: the test data can be saved as OCP trace files and monitoring software, such as OCP Conductor provided by Duolog Technologies Ltd. or other OCP tools, and can be used for test data analysis. ■

Debug Grows Increasingly Critical

By Dr. Neal Stollon, Principal Engineer for HDL Dynamics

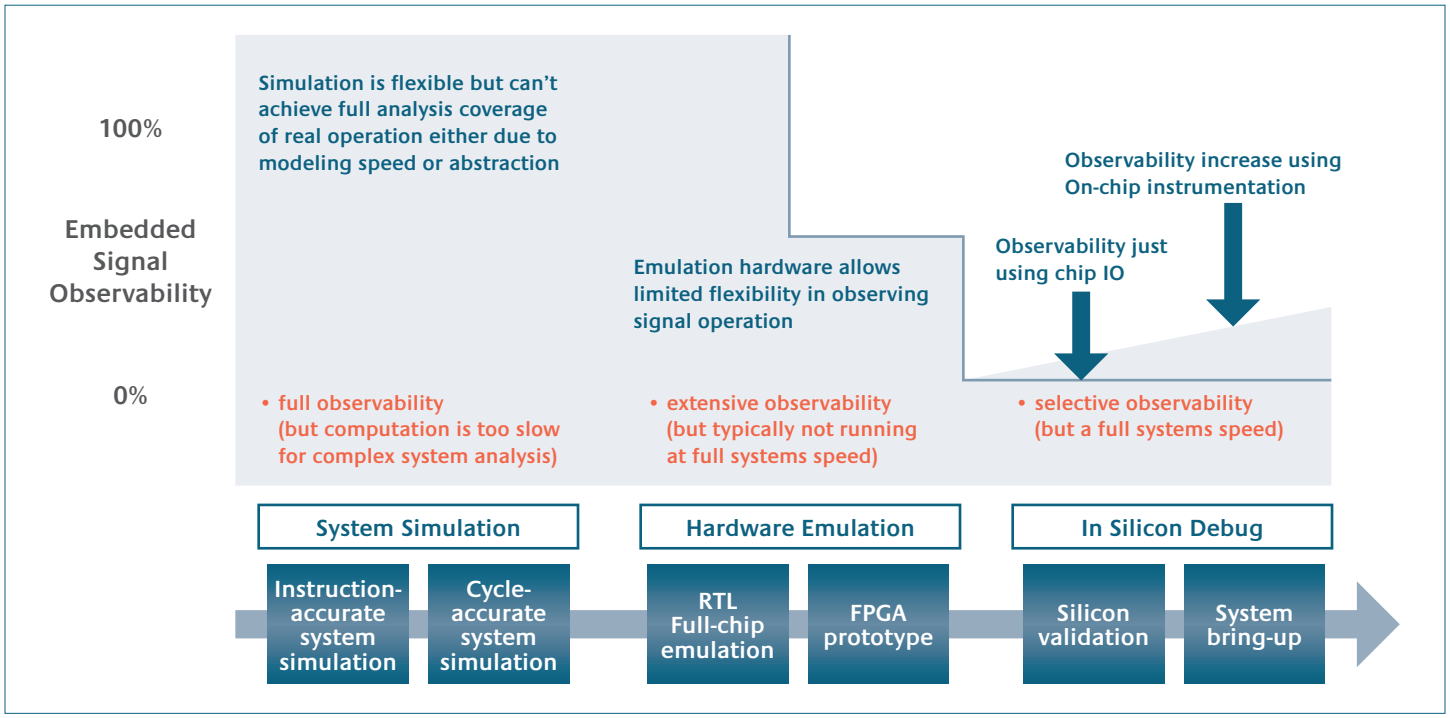
For complex silicon systems, the design team breathes a sigh of relief once the simulations and other assorted analysis are checked off and the chip is sent to the foundry. But the experienced engineers who are involved know that at this point, the job is only half done. The next and possibly most critical stage of verification and analysis happens when the chip gets back from the fab and is bolted on the test fixture. At that point, they start the arduous and often frustrating job of getting the first silicon working. Under the term "debug" are commonly lumped the process of bringing up the silicon as well as all of the tuning, hardware/software integration, and verification that ensure that the system works across the designated environment and interfaces. This area has its own special challenges—not the least of which are due to the lack of visibility and control of what's going on inside complex systems running at high speeds. In recent years, the term "design for debug" has been used to address the range of techniques and approaches that designers can take to improve the visibility and control of testing and analyzing their silicon products.

One of the more common methods of design for debug has been the use of hardware emulators. These emulators allow the observation of embedded signals in hardware while permitting their comparison and validation with simulations. In most instances, however, the emulator operating speeds are too slow to approach anywhere near real-time analysis of operation as it will be in the final silicon.

Other parts of the silicon analysis have been addressed by various design-for-test (DFT) approaches. To a large extent, such approaches rely on tried and true JTAG scan, built-in self-test (BIST), and related embedded test techniques. These techniques have worked well for many designs in providing a snapshot of the chip's operations. With the increased complexity of many multicore, multiprocessor, and multi-subsystem ICs (the proverbial system-on-a-chip or SoC), traditional test approaches tend to break down, and for a number of reasons.

For example, with very-high-speed devices, a traditional test infrastructure may not be able to run at high enough rates to wring out a problem that's only occurring at maximum speeds. Or, problems may be related to specific corner cases of initial conditions or stimulus that aren't fully exercised by BIST. Probably the most critical area of analysis is to understand the specifics and interactions of SoC hardware and software—the testing of which is limited or nil in most DFT strategies. ■

For the complete article, please visit
www.ocpip.org/pressroom/articles/Recently_Published_Articles.



This graphic depicts various approaches to design for debug.

Recent Publications

Available in the OCP-IP Press Room at www.ocpip.org/pressroom.

Press Releases

March 4, 2008: OCP-IP Unveils CoreCreator II

March 3, 2008: OCP-IP Announces Part 1 of Network-on-Chip Benchmarking Specification

January 8, 2008: OCP-IP Announces New Debug Specification

January 7, 2008: OCP-IP Announces Six New Members

January 2, 2008: GreenSocs Wins OCP-IP Outstanding Contributor of the Year Award

Articles

March 6, 2008: Standards Advance for Virtual Prototyping – Smattering of new specs, products in the works – EE Times

March 3, 2008: March 2008 OCP-IP Update for HWS World – EDA Designline

January/February 2008: Debug Grows Increasingly Critical – Chip Design

January 29, 2008: IP – European Style – Embedded Technology Journal

January 14, 2008: Automated Formal Verification of OCP-based IP's Using Cadence's OCP VIP Library – EDA Designline

January 9, 2008: OCP VIP: A Cost Effective and Robust Qualification Process for Multimedia and Telecom SoC Designs – Embedded.com

Announcements

Debug Specification Version 1.0 – Now Available!

The Debug Specification provides a set of guidelines and recommended signal interfaces for on-chip debug of OCP-based systems and related multicore architectures. It provides a framework for IP and tools providers to develop comprehensive and re-usable debug and instrumentation environments that provide on-chip analysis and control features including trace, triggering, multicore synchronization, etc. along with recommendations for integration within ESL environments. The specification can be downloaded here: www.ocpip.org/socket/ocpspec/.

Debug White Paper – Available

The Debug Working Group published a white paper describing an approach to a standardized OCP-bus compliant debug interface based on the Debug Interface Socket. The white paper is available free at www.ocpip.org/socket/whitepapers/.

Network-on-Chip Benchmarking Specification, Part 1 – Now Available!

The specification presents a modeling methodology for applications running on multicore systems and defines an XML format for documenting and distributing NoC benchmarks. It defines a black-box view of the processing elements that discloses only the computational aspects that are relevant in interacting with the on-chip data transport mechanism. The specification can be downloaded here: www.ocpip.org/socket/ocpspec/.

NoC Benchmarking White Paper – Available

A white paper written by OCP-IP's university partners and industry contributors outlines the need for NoC benchmarking as well as the essential features of a NoC benchmarking environment, and drives toward establishing widely accepted and important benchmarks. The white paper is available free of charge at www.ocpip.org/socket/whitepapers/.

SystemC Model 2.2.1 – Available

The System Level Design WG recently released the SystemC Transaction Level Monitor Channel version 2.2.1. Version 2.2.1 is available to both OCP-IP members and the general public on the OCP-IP Web site: www.ocpip.org/socket/systemc/.

OCP 2.2 Specification – Available

The Specification Working Group officially released the OCP 2.2 Specification in January 2007. This version contains an EnableClk feature, support for two-dimensional block burst sequences, non-blocking flow control options, and a security profile. In addition, the verification section has been incorporated into the main specification. For more detailed information, please visit www.ocpip.org.

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