

# OCP-IP News

The Official Newsletter of the Open Core Protocol International Partnership

## Membership Announcements

OCP-IP is proud to announce the following new members:

**AerieLogic** – AerieLogic leverages its extensive experience in industry-oriented formal verification to provide turn-key formal verification solutions to end users, as well as state-of-the-art OEM products for integration by third-party EDA or CAD companies.

**Digital Dynamics Corporation** – Digital Dynamic Corporation is an EDA/ESL company focusing on creation of utility tools and services for electronic design.

**Georgia Tech University** – Georgia Tech is a new addition to the OCP-IP University Community and will be conducting research on System-on-Chip.

**Perfectus** – Perfectus provides cutting edge verification framework technologies for high-speed serial communications and automatic test generation.

**Regulus** – Regulus provides development and design environmental solutions, specific system LSI development, design and software development and verification.

**sci-worx** – sci-worx is one of the world's leading technology licensing and design companies specialized in multimedia and mobile applications. sci-worx combines state-of-the-art design methodology with highly optimized IP-core technology to provide its customers with premier design solutions.

**Silicon Valley PA, Inc.** – Silicon Valley PA, Inc. (SVPA) is an architecture and design solutions company, specializing in System-on-Chip (SOC) architecture, comprehensive design services and training.

**Stream Processors, Inc.** – Stream Processors, Inc (SPI) is a semiconductor company providing high-performance, highly efficient signal and image processors.

**University of Southampton** – The University of Southampton is engaged in research related to System-on-Chip and is a new University Program member.

## Industry Events

### Fall Processor Forum 2006

October 9-11, 2006  
San Jose, California

### Fall Processor Forum 2006

November 7-8, 2006  
Japan

### Electronica 2006

November 14-17, 2006  
Munich, Germany

### IP-SoC 2006

December 6-7, 2006  
Grenoble, France

### OCP-IP

#### Mission Statement:

Promote and support OCP as the complete socket standard that ensures rapid creation and integration of interoperable virtual components.



By Ian Mackintosh  
OCP-IP Chairman  
and President

## President's Overview

Since the last edition of the newsletter, we have continued expanding our industry leadership position through special events across the globe including the US, Canada, Japan and Taiwan, with help from members ITRI and CoWare and through the efforts of our own Marketing Working Group.

The infrastructure surrounding OCP continues to thrive and flourish with the addition of the OCP Property Specific Language (PSL) package to aide in verification of IP blocks. The PSL package compliments traditional verification methodologies, eliminating the need for “best guess” verification by engineers making certain an OCP interface complies with the specification, assuring verification quality and that IP blocks are compatible. This package is again available at no cost to our members.

In addition, Synopsys has announced the release of verification IP for the OCP Interface.

To help our members keep track of the ever expanding infrastructure and support available to them we have developed and introduced a new “Infrastructure Wheel.” The Wheel was developed at the request of members as a way to conveniently outline details and status of the profound OCP infrastructure and deliverables.

As part of the OCP-IP infrastructure, members receive numerous benefits including: free training and support, software tools, and documentation, enabling them to focus on the challenges of SoC design. Leveraging OCP-IP's established infrastructure eliminates the need to internally design, document, train and evolve a proprietary standard and support tools, freeing up critical resources for the real design work and providing enormous cost savings.

Each “spoke” of the wheel diagram identifies content for that particular category of infrastructure. By clicking on each of the major headings shown in the wheel, visitors can readily review all deliverables and content available to OCP-IP members, as well as the current status of any associated workgroups or organizational activity. This website utility was developed to enable readers to quickly and comprehensively understand the already large and rapidly expanding scope of benefits, activities and deliverables available to members. More information about the Wheel can be seen on page 6.

As always, if you have a technical article discussing your use of OCP that you would like published in an industry publication or the OCP-IP newsletter, please email us at [admin@ocpip.org](mailto:admin@ocpip.org).

We want to thank all our members who contributed to this newsletter or to the general success of OCP-IP by making presentations, hosting events and donating to our infrastructure. In every form, your support is greatly appreciated!

Sincerely,  
Ian Mackintosh,  
Chairman and President, OCP-IP

# Working Groups: Reports and Updates

## **Specification Working Group**

The Specification WG has implemented agreed enhancements to the OCP Specification into a draft version of the OCP 2.2 Specification. The OCP 2.2 Specification is currently in member review. The specification is due to be released in December.

## **Technical Vision Working Group**

In March, the Technical Vision WG fully re-examined and prioritized OCP-IP's role within the industry, including supporting infrastructure and benefits to SoC users. All OCP-IP working groups have developed specific roadmaps and goals for work to be completed in 2006, which the OCP-IP Governing Steering Committee will continue to monitor and support throughout the remainder of the year.

## **System-Level Design Working Group**

The SLD WG has been defining the content of the new release (2.1.3) of the OCP channels and monitors. Contributions from CoWare, Greensocs, Sonics, ITRI and TI are being assembled for a release in the near future. The new release also includes a few bug fixes where non-contributing users identified problems. The high quality of the code improves steadily as the user base expands and the pre-release testing procedures benefit from ITRI's regression testing work.

## **Marketing Working Group**

The MWG recently introduced an interactive Wheel infrastructure, outlining the numerous features and benefits of OCP-IP membership. For more information visit <http://www.ocpip.org/membership/information/wheel>.

The MWG also coordinated another successful OCP-IP booth at DAC 2006. The MWG is preparing for upcoming events, including FPF San Jose, FPF Japan, Electronica 2006 in Germany and IP-SoC in France. More information can be found at [www.ocpip.org/pressroom/schedule/speaking](http://www.ocpip.org/pressroom/schedule/speaking).

## **Functional Verification Working Group**

The FVWG is currently reviewing a list of proposed configuration checks to be included as part of compliance. The group is working with the Specification WG regarding the merge of the compliance document into the protocol specification.

The FVWG has outlined the proposed sections, which are currently being reviewed. The group is also reviewing the 2.2 specification to identify additional checks that will be required by the OCP 2.2 updates.

## **Cache Coherence Working Group**

Both the "OCP Coherence Extensions: Part 1, Coherence Framework" document (version 0.6b) and the "OCP Coherence Extensions: Part 2, Signals and Encodings" document (version 0.75) are ready for broader review. Work in creating detailed implementations of master, slave, and interconnect coherence models (as well as, their abstract formal models) has been started; the results will be documented in Part 3 of the OCP Coherence Extensions specification.

## **Debug Working Group**

The OCP-IP Debug Interface Standard pursued a short series of meetings with the OCP-IP Specification WG. In cooperation, the OCP Debug Interface Specification was discussed and a proposal is being prepared for member review.

The Debug Interface for OCP IP-blocks offers a uniform connection for all IP's that have debug capabilities. Moreover, observability of IP-blocks that are not prepared for debugging can be reached by bus observation. In this way, companies can offer OCP bus observation hardware blocks that connect to debuggers outside of the chip and thus display waveform information about bus transactions. In the coming months the group anticipates having a first proposal approved for member review.

## **NoC Benchmarking Working Group**

This group is completing a draft of their initial White Paper on benchmarking and will begin meeting regularly in 4Q06. ■

# Implementing Digital Oscilloscope in Structured ASIC Fabric

Mircea Moldovan, Dan Nicula, Traian Tulbure  
eASIC Corporation

## Introduction

As the development costs for Standard-Cell design in deep-submicron technology approach the multi-million dollar level, it is inevitable that some designers will shift to an alternative solution that can reduce development costs, even if there is some penalty in overall cost or performance.

Structured-ASICs have emerged as this alternative to standard-cell design. Bridging the gap in performance and cost between Standard Cell ASICs and high-density FPGAs, Structured ASICs maintain the best aspects of both technologies. Designers can achieve quicker time-to-market and lower development costs than standard ASICs while also achieving higher performance and lower unit costs than FPGAs.

A subset of the Structured ASIC category is the Programmable ASIC which is via-customizable, rather than metal layer customized. In Programmable ASIC arrays, all metal layers are standard/pre-fabricated, out of which four layers are used for efficient segmented routing, and only a single via-layer is customized to implement a design.

The following case study describes the implementation of a digital Oscilloscope on the eASIC Programmable ASIC fabric. This design is dubbed eScope. It includes a two-channel digital sampling oscilloscope and an arbitrary waveform generator in a single USB-powered module.

eScope was implemented on a 130nm Programmable ASIC device. The chip includes the digital logic (sample buffer memory interpolating digital trigger logic, waveform output buffer memory, data sequencers, and USB IO interface logic) and interfaces to external analog circuitry and USB transceiver logic. A single on-board 80MHz oscillator drives the on-chip PLL clock generators to create separate clock domains for each digital input and output channel, as well as for the USB IO channel.

The eScope is connected to a PC through USB. A PC GUI is used to view and process the acquired data.

The following sections describe the eScope implementation.

## I. Overview

The eScope is a PC-based digital sampling oscilloscope. PC-based oscilloscopes offer real cost savings over desktop oscilloscopes. One can use the existing large color display, fast processor and large disk storage of the PC instead of having to buy a stand-alone oscilloscope.

Digital sampling oscilloscopes use the equivalent-time sampling method to capture and display signal samples. Sampling oscilloscopes can measure signals up to an order of magnitude faster than real-time oscilloscopes. As such, these oscilloscopes are ideal tools for capturing and characterizing computer, datacom and telecom signals.

## II. eScope Architecture

The eScope design is implemented using nine sub-modules and uses Open Core Protocol (OCP) to interconnect a common shared memory to various data access ports. The sub-modules are:

- clkGen: clock/reset generator for eScope
- adclnput: synchronizers for the data samples from ADC
- dacOutput: FIFO synchronizers for the waveform data to DAC
- trigGen: trigger generator includes an OCP initiator port
- waveGen: waveform generator logic includes an OCP initiator port
- hostIf: USB module host interface includes an OCP initiator port
- sampleMem: block memory shared for storing data samples and wave generator data
- ocpMerge: 3:1 combinatorial OCP merge
- ocp2mem: OCP to memory interface converter, includes an OCP target port

For the full article, please visit the OCP-IP website at: [www.ocpip.org/pressroom/articles/Recently\\_Published\\_Articles/](http://www.ocpip.org/pressroom/articles/Recently_Published_Articles/). ■

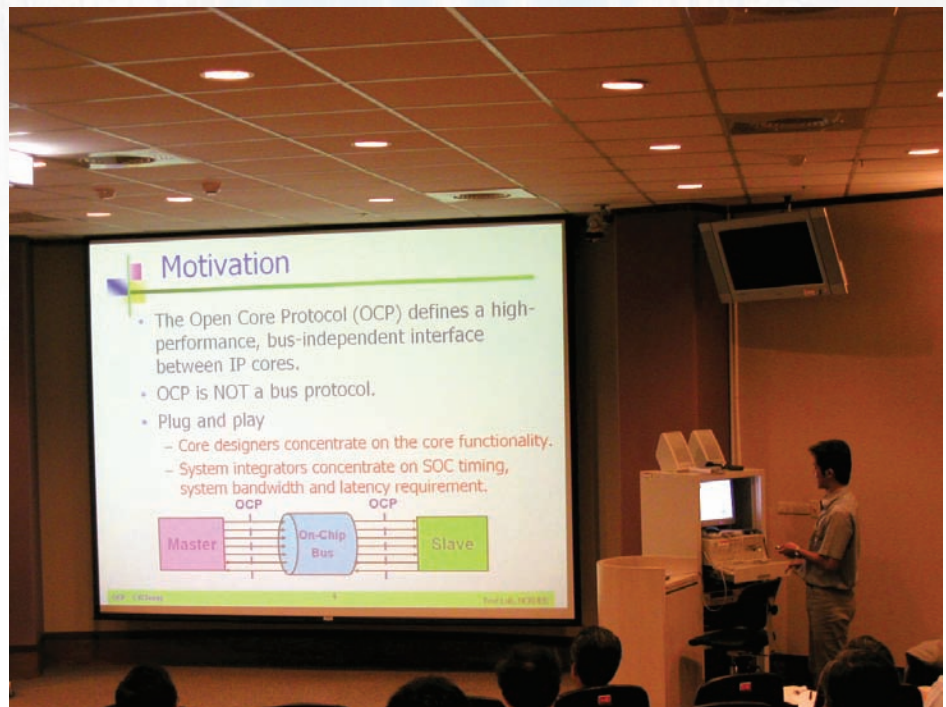
# OCP-IP Presentation at the CoWare ESL Show



OCP-IP participated in CoWare Japan's "CoWare ESL Show" held in Tokyo this past August. The August 25th event was attended by over 120 engineering specialists working in the area of developing SystemC platforms for SoC architectural development and verification, and early software development. Covering not only OCP-IP's introduction and vision, the Keynote presentation entitled "OCP-IP: Supporting ESL" reviewed the activities of the OCP-IP System Level Design Working Group (SLDWG), including the excellent collaboration work on the Open SystemC Initiative (OSCI). Standing in for OCP-IP President Ian Mackintosh (who had been looking forward to the trip to Tokyo, but had to bow out at the last minute due to urgent medical reasons), CoWare's Tim Smith, vice president worldwide sales, delivered the presentation with style and gusto.

Definitions of TL1 (word and cycle accuracy), TL2 (burst level and word level timing accuracy) and TL3 (packets and total event ordering accuracy) were presented so that the modeling experts in attendance could best comprehend the tradeoffs of modeling accuracy and simulation speed. The popular "SLDWG Package" (downloads of >3500 to date) featuring a highly-configurable channel, adaptors between abstraction levels, a monitor for performance analysis and over 130 pages of documentation was described.

Since this was a CoWare-sponsored event, there was discussion on how CoWare's flagship SoC architecture platform modeling environment, Platform Architect, supports the TL1, TL2 and TL3 levels of abstractions. CoWare's Architect's View Framework bus library, which contains point-to-point channels, simple shared busses and Network-on-Chip cross connect models, were also discussed. Lastly, a TI OMAP-based, real-world platform example, showing how OCP-IP and SystemC TLM can be combined to create high-speed SystemC TLM platforms based on standards that are scalable, was presented.



The "OCP-IP: Supporting ESL" presentation is available in the OCP-IP Pressroom at [www.ocpip.org/pressroom/schedule/speaking/](http://www.ocpip.org/pressroom/schedule/speaking/). ■

# Network on Chip Benchmarking Initiative: a Snapshot on the Who, the What and the Why

Cristian Grecu  
University of British Columbia

Networks-on-Chip (NoCs) are generally viewed as the ultimate solution for the design of modular and scalable communication architectures. NoCs provide support to the integration of heterogeneous cores through the standardization of the network boundary. NoC architectures are effective at mitigating the delay limitations in signal propagation across deep-submicron interconnects and can significantly improve design predictability and shorten the design cycle.

Numerous groups in industry and academia are working towards providing solutions aimed at NoC design flow components, including architectures, protocols, mapping algorithms, simulation environments, etc. However, due to the multitude of design parameters and trade-offs involved, it is virtually impossible to compare two different NoC platforms. Performance figures are meaningless if not accompanied by an exhaustive description of assumptions, design choices and experimental setup. To advance and accelerate the state of the art of the NoC paradigm R&D, the research community is in need of widely available reference benchmarks that allow a sensible comparison.

OCP-IP members from the University of British Columbia (Canada), Royal Institute of Technology (Sweden), Carnegie Mellon University (USA), Tampere

University of Technology (Finland) and Washington State University (USA) have joined forces to lead this ambitious initiative. Their objective is to provide a set of benchmarks aimed at the full NoC design flow, ranging from design specifications and performance evaluation to testability and fault tolerant features. As such, the major directions currently pursued by members of the Network-on-Chip Benchmarking Initiative are focused on the following three themes:

- application modeling and design metrics for NoC benchmarking;
- micro benchmarks for exercising and analyzing specific features of NoCs;
- benchmarking methodologies for assessing testability and reliability of NoCs.

The founding group of this initiative is seeking contributions and participation from other interested parties. In particular, at this stage, we are specifically looking for NoC hardware descriptions and high level application data relevant to benchmarking activity. Please provide us with comments and viewpoints on our efforts. Better still, formally join our group to participate and lead the directions of this initiative. Please contact OCP-IP at [admin@ocpip.org](mailto:admin@ocpip.org) or Cristian Grecu at [grecuc@ece.ubc.ca](mailto:grecuc@ece.ubc.ca) for more information. ■

## OCP-IP Wheel Infrastructure

OCP-IP recently introduced an interactive Wheel, outlining the OCP-IP infrastructure and deliverables. Each spoke of the wheel diagram identifies the content for that category of infrastructure. Each of the major headings shown in the wheel identifies features available to OCP-IP members and the current status of any associated workgroups or organizational activity. This page was developed to enable readers to quickly and comprehensively understand the already large and growing scope of benefits, activities and deliverables available to our members.

The Wheel can be viewed on the OCP-IP website at [www.ocpip.org/membership/information/wheel](http://www.ocpip.org/membership/information/wheel). ■



# NoC Benchmarking Activities at Tampere University of Technology

Erno Salminen, Research Scientist  
Tampere University of Technology

Although benchmarking has a long history in microprocessor and CAD tool design, it has just recently gained attention in Network-on-Chip (NoC) research. NoC Benchmarking Workgroup (NoCBW) is a collaboration of universities aiming to provide a set of characteristic benchmark designs that help the development and deployment of the NoC paradigm. Such a set allows comparison between NoC proposals, which is not possible when proprietary, non-documented test cases are utilized. This enhances scientific credibility, as the new claims and solutions are more easily reproduced and justified by other researchers. At the same time, common guidelines for performance and cost evaluation methodologies are needed.

Advanced FPGA technology has recently enabled rapid, cost-effective single-chip multiprocessor design and prototyping. This enables execution of actual applications in real-time at the cost of reduced visibility compared to simulation. Full synthesis, placement, and routing phases are naturally required and, therefore, the evaluation of conceptual methods must be done with simulators. In our experience, FPGA-prototyping with real software is a crucial step. Firstly, to ensure correctness and secondly, to account for subtle effects, such as cache misses, busy wait penalties and interrupt latencies. Otherwise, the results obtained from simple simulations might be too optimistic. For example, the full potential of a network may be impossible to achieve in reality, unless all the parts (application code, custom logic, memory hierarchy, etc.) are carefully selected and optimized. Currently, we have a working 16-PE multiprocessor system on a single FPGA running at 100MHz. The results with data-parallel MPEG-4 video encoding are very promising and, to our knowledge, state-of-the-art. Work is in progress to measure the performance with various network topologies.

For the full article, please visit [www.ocpip.org/pressroom/Adoption\\_Stories](http://www.ocpip.org/pressroom/Adoption_Stories). ■

#### Further information:

DACI research group: [http://www.tkt.cs.tut.fi/research/daci/daci\\_overview.html](http://www.tkt.cs.tut.fi/research/daci/daci_overview.html)

NoCBWG: <http://www.ocpip.org/wiki/university/FrontPage>

# ITRI ESL Working Group Presentation

The ESL Working Group of Taiwan SoC Consortium gave a presentation on the OCP Specification in the 5th Working Group Meeting held on August 24th at Conference Room 9-010, Industrial Technology Research Institute, Hsinchu, Taiwan. The speaker was Mr. Chin-Yao Chang, a researcher working with Professor Kuen-Jong Lee of National Cheng Kung University, Taiwan. The talk covered the OCP Specification in terms of the protocol and the layered hierarchy from system to RTL level. An example illustrating the transactions among masters and slaves with OCP was provided.

The group of attendees varied from design houses, universities, research institutes and EDA houses.



#### Design houses:

Faraday, Ya-Ra Information, Avery Design Systems, IP Lib and JMicon

#### Universities:

National Cheng Kung University and National Tsing Hua University

#### Research Institutes:

ITRI and National Chip Implementation Center (CIC)

#### EDA houses:

Springsoft, CoWare and Avant ■

## Recent Publications

Available in the OCP-IP Press Room  
at [www.ocpip.org/pressroom](http://www.ocpip.org/pressroom)

### Press Releases

September 19, 2006: OCP-IP Introduces New Infrastructure Wheel

September 13, 2006: Synopsys Releases Verification IP for the OCP Interface

July 11, 2006: OCP-IP Releases PSL Package

### Articles

August 25, 2006: MP: SoCs: What are the Tools?

July 19, 2006: Processor Model Aims to Unite Design Flow

July 17, 2006: Vast Adds Performance, Power Enhancements to Flagship Tool

July 12, 2006: How to Implement a Digital Oscilloscope in Structured ASIC Fabric

July 10, 2006: Transactor Library Eases System-Level IP Incorporation

July 10, 2006: Novas Makes Transaction-based Analysis More Accessible to HDL Users

July 7, 2006: Firm's Initiative Targets SystemC IP Interoperability

## Announcements

### OCP PSL Package—Now Available

OCP released a Property Specific Language (PSL) package to aid in verification of IP blocks. The PSL package compliments traditional verification methodologies eliminating the need for “best guess” verification by engineers. This certifies that an OCP interface complies with the specification, assuring verification quality and that IP blocks are compatible.

### Native SystemC Assertions Package—Now Available

NSCa is a native C++ assertion product that easily integrates to SystemC and provides a natural

verification extension to the current SystemC 2.1.2. NSCa facilitates the discovery of bugs at the system level design phase and assures functional models are correct before methods like high-level synthesis or system to RTL equivalence checking are used. This results in time and cost savings by speeding bug discovery at the system level before propagation to RTL.

### 2.1.3 SystemC Models—Available in October

The System Level Design WG is preparing a release of the OCP SystemC TLM channel version 2.1.3. The new features improve model interoperability, resulting in better productivity in system level modeling. In addition, OCP-IP announced the donation of a regression suite to the organization by the Industrial Technology Research Institute (ITRI). The regression suite enables OCP-IP to ensure a superior level of code testing before releasing the Channel.

### OCP CoreCreator 4.0 Training—Available

The OCP training for CoreCreator 4.0 is available to OCP-IP members. To request your copy of this training please contact [admin@ocpip.org](mailto:admin@ocpip.org). (Please include complete shipping information).

### OCP 2.1 Training—Available in Japanese

OCP 2.1 training in Japanese is available to OCP-IP members. If you would like to receive your copy, please send a request to [admin@ocpip.org](mailto:admin@ocpip.org). (Please include your complete shipping information).

### OCP Technical Support—Available in Japanese!

OCP technical questions in Japanese can now be accepted by e-mailing [jptech@ocpip.org](mailto:jptech@ocpip.org).

### OCP 2.1 Training—Available

Training for the OCP 2.1 Specification is available to OCP-IP members. To request a CD of this training please contact [admin@ocpip.org](mailto:admin@ocpip.org). (Please include your complete shipping information).

To request additional copies of this publication, contact [admin@ocpip.org](mailto:admin@ocpip.org)



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