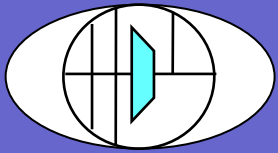


OCP-IP Debug Status and Plans

System, Software, SoC and Silicon Debug S4D Sept. 25, 2009

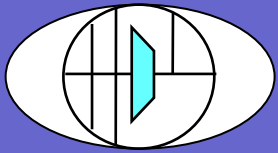
Dr. Neal Stollon, HDL Dynamics

neals@hdldynamcs.com

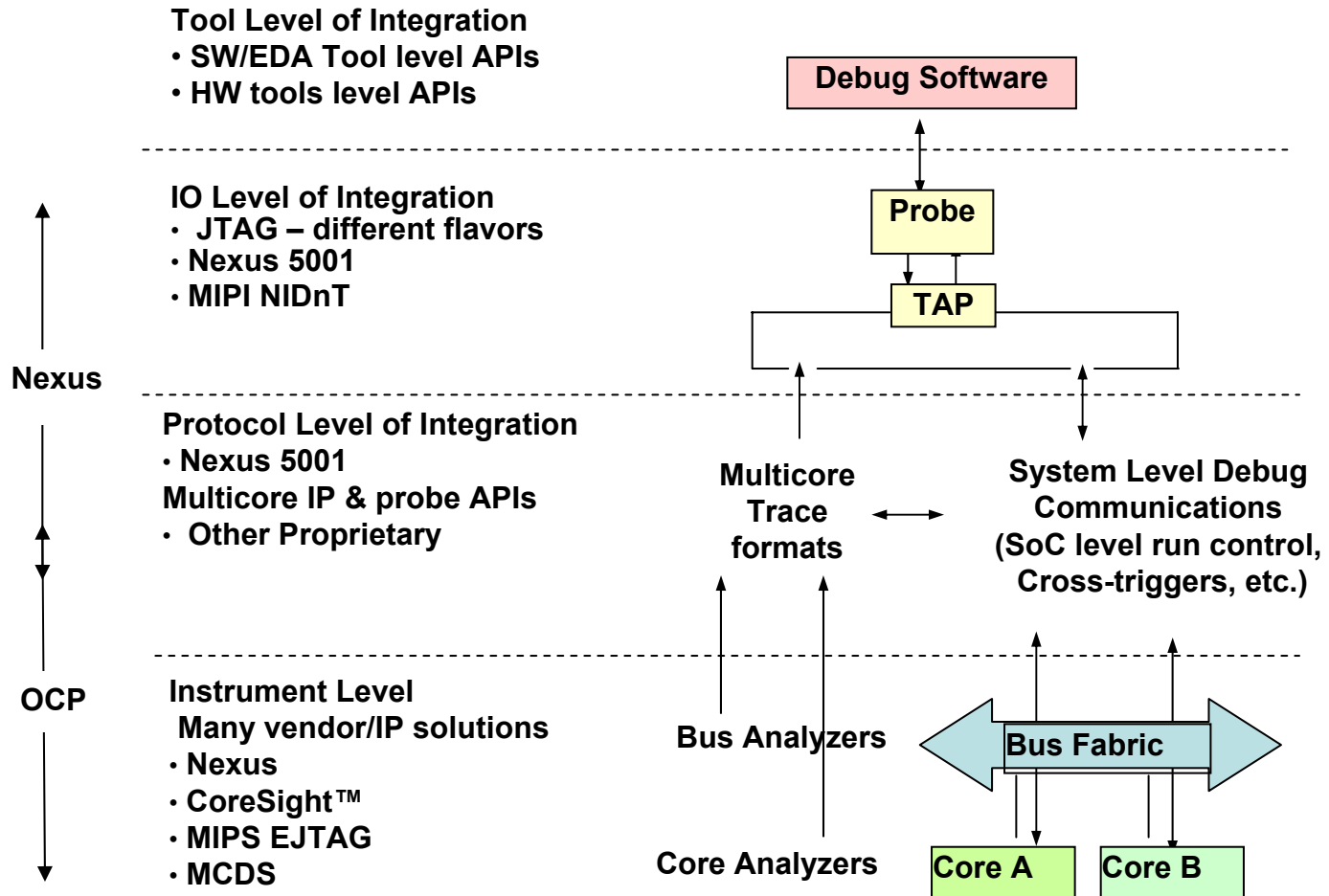


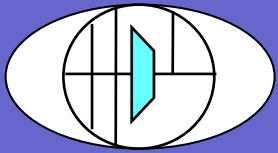
SoC Debug Issues

- **Debug and trace is crucial to embedded design success**
 - **Difficult to fix what you can not see**
- **System on Silicon Debug Requirements**
 - **Visibility into non-observable sub-system interfaces**
 - **flexible on-chip triggering, trace, performance analysis**
 - **Interoperability with processor debug capabilities**
 - **cross-triggering, common synchronization**
 - **Keeping pace with internal signal speeds**
 - **don't add to timing closure issues**
 - **Reasonable gate size**
 - **configurable to system requirements**
 - **Low IO requirements**
 - **leverage existing debug interfaces**



The Debug Landscape

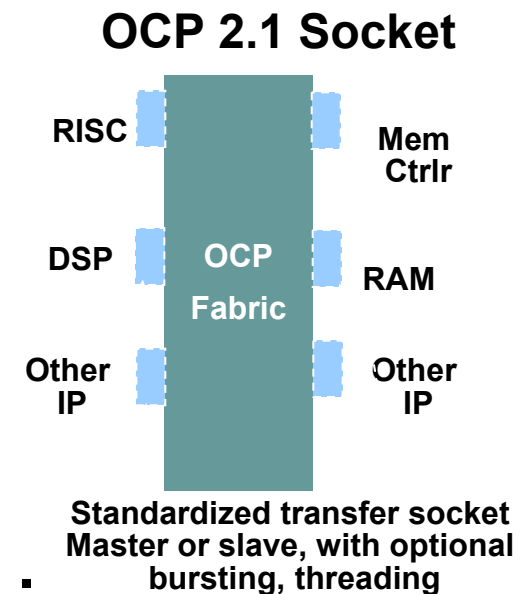


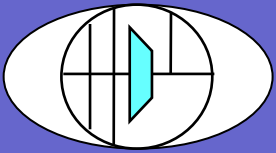


OCP-IP Overview

- Open Core Protocol (OCP) is open standard for intellectual property (IP) core interfaces, or sockets,
 - "plug and play" SoC design
 - Widely used
- IP is International Partnership - . consortium supporting OCP
 - 50+ active members
 - tools, IP infrastructure
 - Working groups in ESL, **debug**, . . .

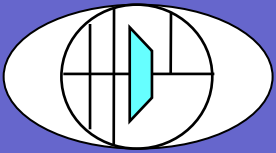
see www.ocpip.org





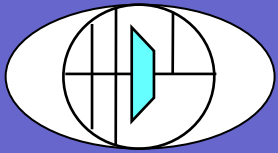
OCP General Features

- **OCP supports range of sophisticated bus interface capabilities ...which also translates into a lot of bus complexity**
 - **64-bit read and write data busses**
 - **32-bit multiple mode addresses**
 - **Multiple Outstanding transactions**
 - **Multiple Command and Response types**
 - **Multiple User defined signals**
 - **Single or Bursted Reads and Writes**
 - **Single Request Multiple Data**
 - **Multiple synchronous core to bus ratios**
 - **Data Ordering and reordering using tags**
- **Bus visibility helps get complex applications running right**



Debug Socket for Multi-Core Debugging

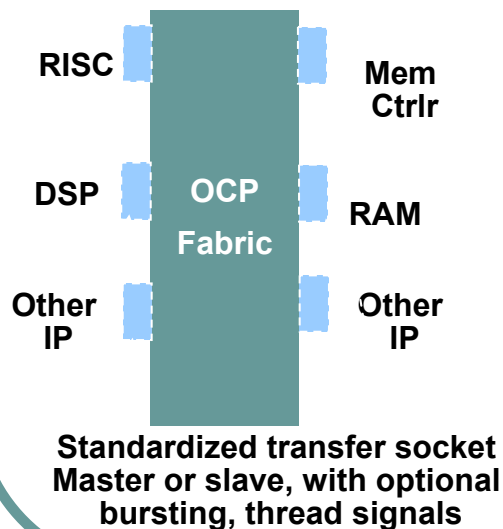
- **OCP-IP Debug WG announced the release of its Debug Standard 1.0 in 2007**
 - **Basic and Extended sets of socket level debug signals**
 - **SoC level Interface uses standard 1149.1 JTAG/ 5001 Nexus**
 - **Debugging of multiple processor cores connected with OCP interface.**
 - **Allows designers to distribute debug signals as part of system interface scheme**
 - **Ability to set up multi-core debug hardware and software using standard signal interfaces**



OCP Debug Working Group

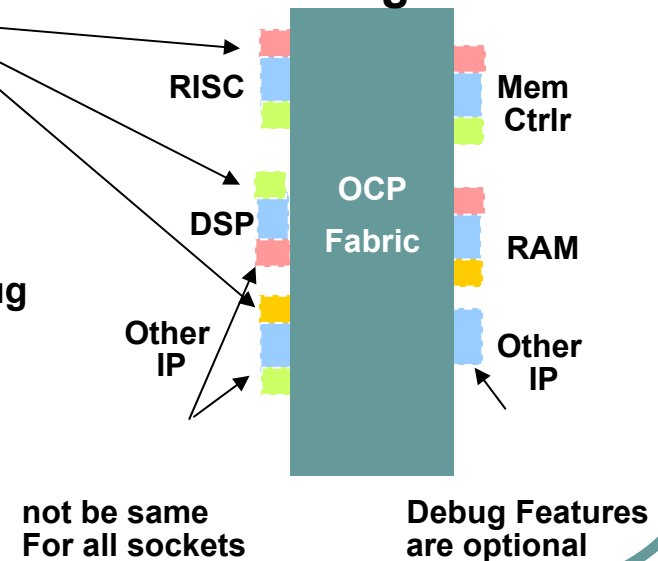
- OCP is neutral On Chip Protocol for SoC IP connection
- WG focus on defining debug related signaling between cores and other embedded subsystems
- Leverage other work for IOs (JTAG, Nexus), APIs, etc.
- Defined subset architecture for on chip debug

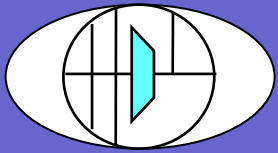
OCP 2.1 Socket



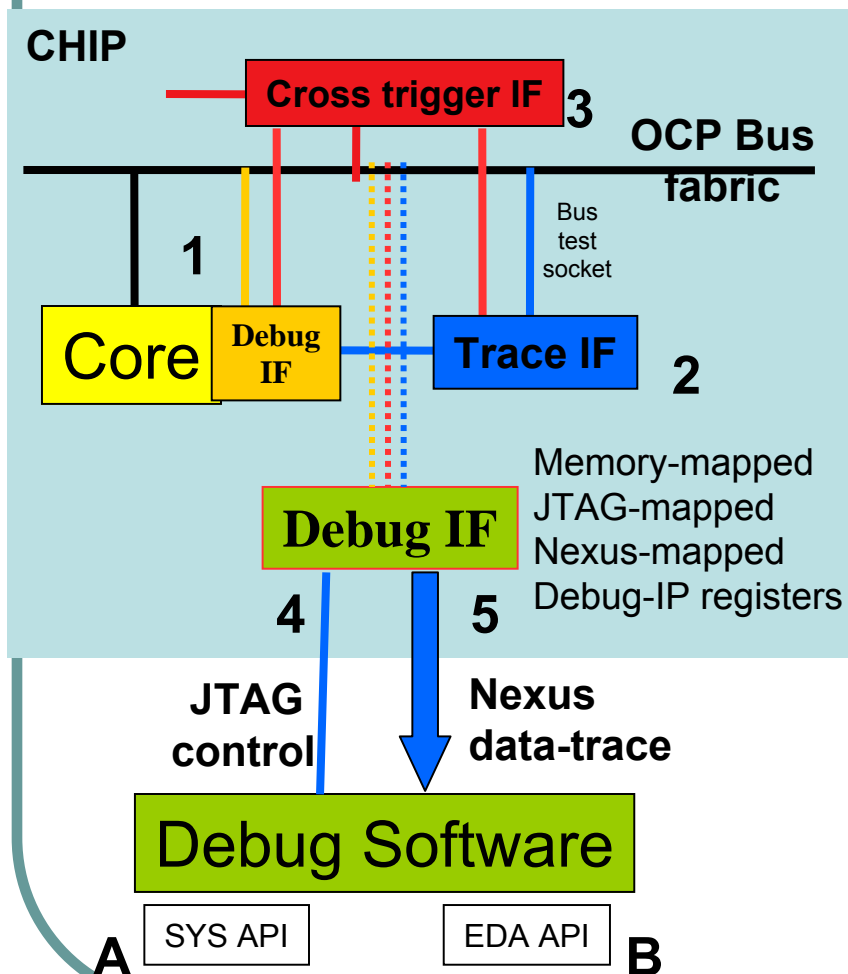
Baseline Sockets
1149.1 JTAG
Debug resets
Generic Processor
debug handshakes
Cross Trigger Interfaces
Synchronize Trace/Debug
Trace Triggers
TimeStamp Interfaces
Power Management
Debug Security

OCP Debug Socket





Debug Hardware Environment

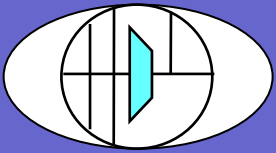


Debug-IP HW connections to SoC:

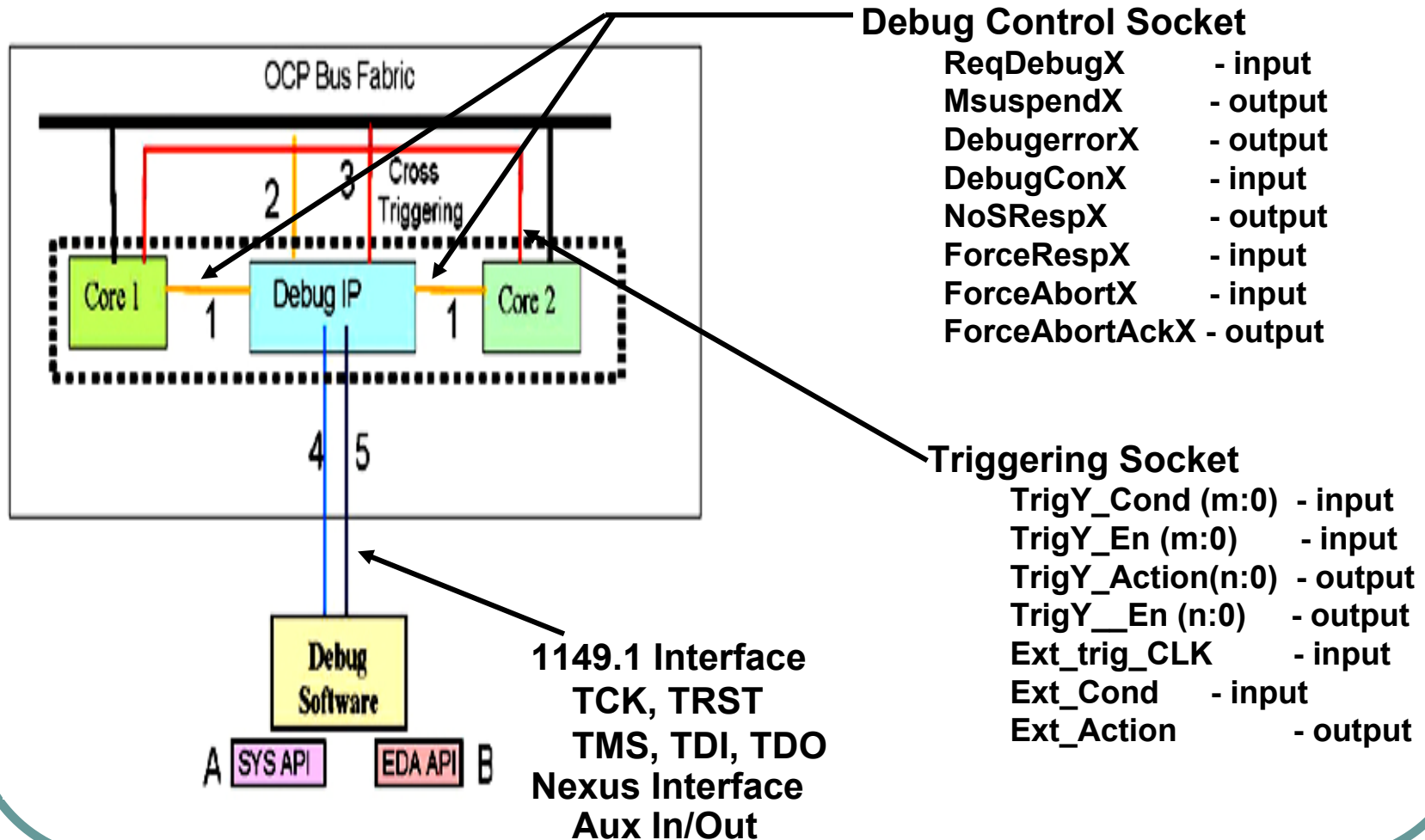
- 1 CORE-INTERFACE:** interfaces to core IP-block debug data/control proprietary IO
- 2 BUS-INTERFACE:** interface to a bus traffic [event/trace data collect, compression and triggering]
- 3 CROSS-TRIGGER INTERFACE:** to other debug-IP blocks [event-synch.]
- 4 PIN-INTERFACE CONTROL:** IF to JTAG for debug control to analyzer/debugger software.
- 5 PIN-INTERFACE DATA:** interface for high speed data [like Nexus]

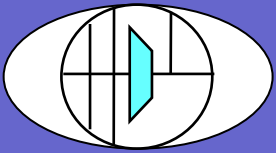
Debug software API for information transfer and display:

- A. System Debug SW API interface**
- B. EDA API interface – block / system level verification (ESL, RTL)**



OCP Debug Hardware Basic Socket





What is in the Debug Specification?

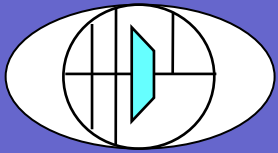
OCP Interface for Basic Debug Signals

- **Debug Control and Run Control for Cores**
 - **Consistent (multiple) processor software debugger interfaces**
- **Cross-Triggering between Multiple Cores and Events**
 - **Scalable to on-chip/off-chip cross triggering**
- **Trace Interface**
 - **Bus traffic observation (system trace) and control (triggering)**
- **New classes of debug errors (different from system errors)**

OCP Interface for Extended Signals (Special features)

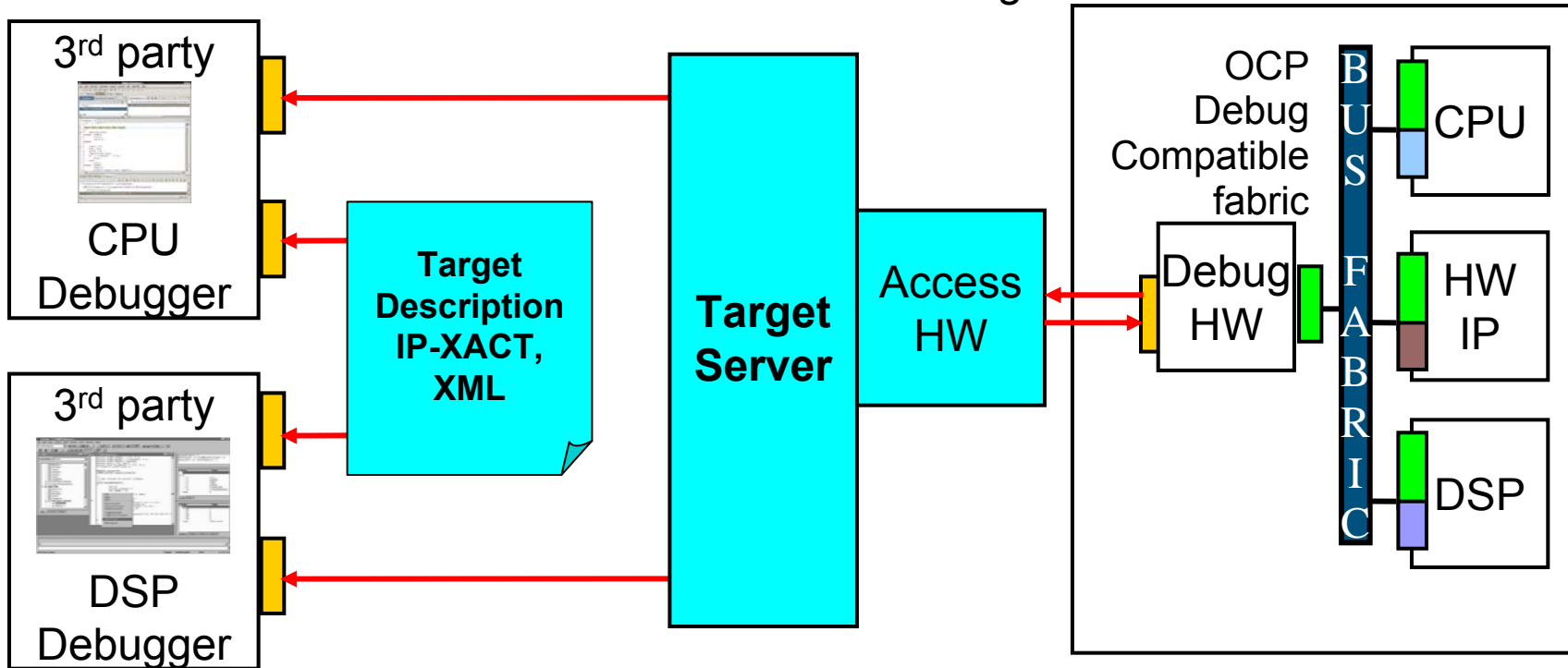
- **Performance Monitor**
- **Time-stamping**
- **Power Monitoring voltage islands, gated clock islands**
- **Security islands**

Of huge value
in final silicon

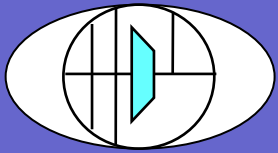


OCP Debug Standard

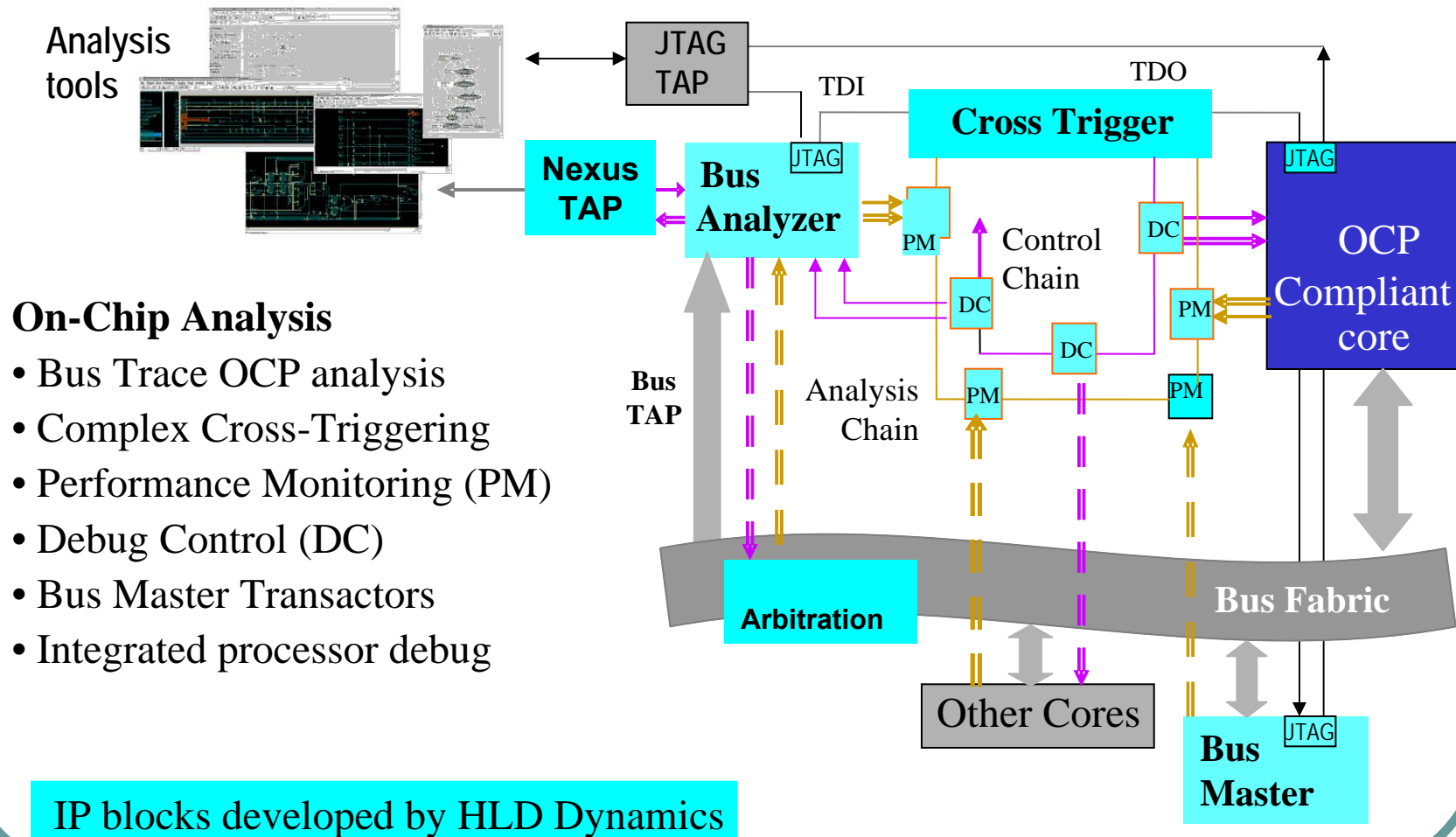
Standard Debug API (SPRINT) Basic OCP Debug Interface Extended OCP Debug Interfaces

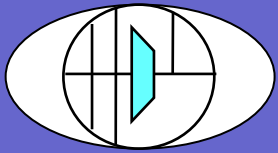


The SPRINT API supports a general debug description for multiple processors.



System Debug Instrumentation OCP Example





OCP Debug Standard Advantages

Simplifies debug - Standardized Basic OCP core Debug Socket

Facilitates Debug Hardware and debugging Software offered as standard IP

Opens implementation and support of (heterogeneous) processors

Proprietary Debug solutions supported - Need just OCP Debug wrapper

Fixed OCP debug interface, compatible to multitude of debug interconnects (i.e. Nexus, serial buses, cross bar, NoC, etc)

High initial uptake of the new standard in the OCP-IP community