

OCP-IP News



Membership Announcements

Imperas - providing the infrastructure for the future of software virtual platforms and enabling the next generation of embedded software development



InfoComm Research Institute - The Institute for Infocomm Research is a member of the Agency for Science, Technology and Research (A*STAR) family. Established in 2002, our mission is to be the globally preferred source of innovations in 'Interactive Secured Information, Content and Services Anytime Anywhere' through research by passionate people dedicated to Singapore's economic success. I2R performs R&D in information, communications and media (ICM) technologies to develop holistic solutions across the ICM value chain.



Institute for
Infocomm Research

Samplify - a venture-funded solution provider of signal compression technology and semiconductor products. Headquartered in Santa Clara, CA, Samplify's customers include medical imaging and wireless infrastructure companies. Samplify's technology and semiconductor



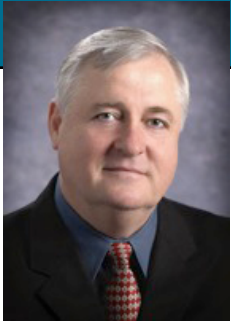
products, have won multiple industry awards for innovation. Additional information about Samplify can be found at www.samplify.com.

This fall, the Electronic Chips & Systems design Initiative (ECSI) will host the **Forum on Specification and Design Languages (FDL)** devoted to the dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modeling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems. This year, the FDL conference will be held alongside the **System, Software, SoC and Silicon Debug, conference (S4D)** conference in Southampton, UK, September 14-16. S4D covers a wide range of issues including the improvement of electronic product quality and reducing product delays.

ECSI will also host DASIP, the conference on **Design and Architectures for Signal and Image Processing**, October 26-28 in Edinburgh, Scotland. The conference program will include keynote speeches, contributed paper sessions, and demonstrations. Special sessions will be held on the topics of: reliable multi-processor scheduling and HW/SW resource management, reconfigurable computing architectures, image and signal processing on GPU, reconfigurable video coding (RVC), and smart image sensors.

ECSI has also launched a new website. The modern, clean and easy-to-use format follows the main ECSI strategy to offer better and more valuable services to members and the Electronic System Design community as a whole. With more than 1,000,000 hits last year, ECSI is building on the synergy of R&D activities among all industry sectors and academia, while increasing value to member organizations. The growing ECSI Resource Center constantly provides access to technical papers presented at the ECSI conferences and other workshops organized by ECSI. It also offers open material from R&D projects in which ECSI is involved. ECSI Members can benefit greatly from privileged access to preliminary results from these projects. More information can be found at www.ecsi.org.

President's Overview



Ian Mackintosh
OCP-IP President and Chairman

Welcome to this edition of the OCP-IP newsletter. We are excited to bring you the latest news regarding the Organization and there is much to tell. In addition to our advanced interface, OCP-IP continues to expand our complete infrastructure for users. Our extensive environment saves members hundreds of thousands of dollars per year and guarantees best-of-breed solutions endorsed by OCP-IP. Our working groups are hard at work behind the scenes and continue to be extremely productive. Most, if not all of the groups are scheduled to release new deliverables and / or updated specs within 2H 2010. It would be remiss not to take this opportunity and once again thank all our working group chairs, as well as our participating members, for their valued contributions making these deliverables a reality. It is through their dedication, support and effort that these deliverables are available and shared between our members.

Our Metadata working group recently released a package of generic Vendor Extensions for [IP-XACT](#). These Vendor Extensions provide a way to fully describe configurable interfaces, (such as OCP) in machine-readable XML structure in an IEEE standard format. They are compatible with both [IEEE1685](#), and IP XACT 1.4. The package is available to both OCP-IP members and non-members alike. Members may access the OCP Metadata Vendor Extension package by completing the online click-through [Commercial Metadata Vendor](#)

[Extension License](#). Non-Members may access the package via an online click-through [research license](#).

Our System Level Design Working Group (SLDWG) continues work on a virtual platform. A Virtual Platform is created by integrating together software-models of different IPs and is used to simulate the functionality of an entire SoC. For more information, please see the [detailed Virtual Platform Article](#) on page three of the April edition of the OCP-IP Newsletter. In addition, the group continues check out of yet another design tool member donation expected for release to the general membership in Q3. As a reminder to everyone, OCP-IP's SystemC OCP TLM Kits fully support the modeling proposed in [OSCI 2.0](#). Members can receive their copy of the Kit by completing our click-through [Commercial License Agreement](#). Non-Members can get copies (without Monitors) by completing the [Research License Agreement](#). The kit represents the first, and most advanced TLM-2.0 based, industry-proven kit in existence today.

Our NoC Benchmarking Working Group has recently submitted their Transaction Generator (TG) to the GSC for approval to publish in Q3. In addition, the Group has been working on a memory modeling technical article, and hopes to prepare other technical articles about the TG during the summer.

OCP and Verification of Configurable OCP Interfaces

Carlo Del Giglio, Senior Applications Engineer, and Alok Sanghavi, Technical Marketing Manager
Jasper Design Automation

The Open Core Protocol (OCP) is a core-centric protocol that comprehensively describes the system level integration requirements of intellectual property (IP) cores. The flexible nature of the specification makes it widely applicable to many different hardware applications that require a simple, robust data transfer protocol. The OCP International Partnership, a group that is dedicated to proliferating the OCP standard, confirms that OCP has been used in numerous SoC designs which have already shipped in many billions of units. The popularity of this protocol continues to increase as more designers become aware of the benefits of a flexible, standard, design socket.

Naturally, along with the advantages of flexibility come many variants of the implementation that fall under the official protocol specification. While this makes it easy to adapt the protocol to the individual requirements of a specific design implementation, it does present a challenge for the verification team. Verifying protocol interfaces is a challenging exercise for any group. Formal verification of protocols has become far more prevalent in recent years because of its ability to exhaustively remove all doubt of incorrect interface behavior prior to tape-out. This article presents a basic overview of OCP, exploring both the basic operation and configuration files. It then introduces a configurable OCP formal verification IP

generator that automatically creates appropriate OCP properties for a specific to design implementation of the protocol. These concepts are used to demonstrate a silicon-tested method of developing a verification plan for OCP designs.

OCP Overview

OCP uses a master and slave configuration. All signals are synchronized on the rising-edge clock. It uses a read and write command structure to pass information between components. It supports both blocking and non-blocking forms, along with basic pipelined operations. The specification is completely bus-independent, with device selection and arbitration performed outside the OCP logic.

Figure 1 illustrates a conceptual implementation of a simple system containing a wrapped bus and three IP core entities: one that is a system target, one that is a system initiator, and an entity that is both.

Multiple read and write commands make up the basic command structure of the protocol. Read (non-blocking), ReadLinked (blocking), and ReadExclusive (blocking) are some of the more common read commands. The write command also contains several forms, including Write (non-blocking), WriteNonPost (blocking), WriteConditional (blocking), and

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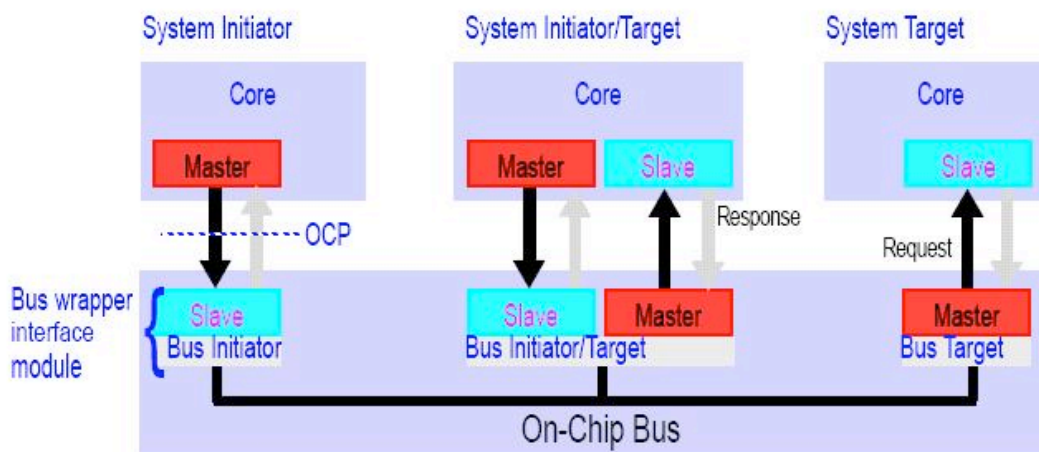


Figure 1. Wrapped Bus with OCP Instances

Broadcast (linked multi-device). OCP signals are divided into three main groups: dataflow, sideband, and test. Basic operation requires only a small subset of the dataflow signals. The sideband and test signals are optional in this configuration.

Because of the many possible configurations for OCP, the specification requires the protocol interface be defined within a text-based configuration file. This file identifies the design-specific parameters such as data command subsets and modes, data and address widths, burst sequence and alignment, data handshaking, and optional signals. The parameters can be explicitly declared in the file or loaded from default settings. *Figure 2* shows a sample configuration file.

The Challenges of OCP Verification

The configuration file provides great flexibility for customizing the OCP details for a specific architecture. In its simplest form, OCP contains only two signals, while the complete specification contains greater than 50. Such variety in the protocol interface creates flexibility for integration, but that flexibility introduces challenges for verification, particularly when considering verification IP reuse goals.

The OCP specification does contain standard property sets for protocol compliance, and several vendors have created pre-packaged property sets based upon this description. In practice,, many of the properties in the specification are simulation-centric by design and are not modeled appropriately for other verification technologies such as formal analysis. Formal verification provides the highest confidence level in verification

today, and protocol verification is an ideal application to benefit from its strengths. Verification teams with access to OCP verification kits not only reduce their verification cycle time, but also increase their confidence in the design behavior rather than just running simulation alone.

Most pre-packaged OCP verification kits exhibit another challenge beyond formal compatibility. The high degree of configuration freedom in the protocol makes it necessary for engineers to determine which properties in the verification sets are meaningful for the design and which can be safely ignored. If this effort is not performed up front, a significant portion of the properties might fail during verification. Debugging these properties on a live design can result in significant verification cycles spent simply trying to determine whether a given failure is reasonable. Understanding what can be safely ignored requires knowledge of what parts of the protocol checking are not required for the particular design under test. The time saved by using a pre-packaged set of OCP checkers can easily be lost or exceeded in the resulting debugging effort if the property set is not well matched to the level of OCP implementation. Engineers who have had to endure this process in the past often consider this to be one of the most difficult issues in using pre-packaged kits. A better solution is needed.

Simplifying the OCP Verification Effort

In an ideal situation, a verification engineer has access to a property set relevant to the particular implementation of OCP in the design under test. A property generator creates a subset of the entire protocol automatically, based upon the design information. The setup is straightforward, without necessitating deep understanding of the protocol and requires few manual changes to the property set once completed. In this preferred situation, the resulting output is not restricted to a specific design or property language, and it is optimized for formal analysis. Jasper Design Automation provides such a capability via JasperGold's OCP proof kit IP Generator.

The tool produces OCP property suites tailored for specific OCP configurations. Functionality outside a specific OCP configuration is not incorporated in the resulting output files. The IP Generator leverages the information within the OCP configuration file to tailor the generated properties to only those that are relevant to the specific design under test. Run times are nearly

```
module top {
  addr_def "" {
    base_addr 0xB
    size 0x1FFF
  }
  interface "internal" bundle "ocp2" revision 1 {
    interface_type slave
    param addr 1
    param addr_width 13
    param enbl 1
    port Sclk net Clk
    port MAddr net MAddr
    port MCmd net MCmd
    port MData net MData
    port STagID net STagID
  } # close interface top definition
} # module close
```

Figure 2. OCP Configuration File

OCP and Verification of Configurable OCP Interfaces (Continued)

instantaneous, and the resulting output files are available in Verilog or VHDL flavors. The IP Generator supports property specification in either PSL or SystemVerilog Assertion (SVA) format. This support provides flexibility not only for use on internally developed OCP blocks, but also with purchased design IP configurations, since you can generate equivalent property sets for mixed-code environments.

When using the IP Generator, engineers do not need to be experts in the overall OCP specification because the resulting property set is automatically minimized using existing design files. Moreover, the proof kit generates properties that are optimized for formal analysis, ensuring the most powerful tools for verification confidence are accessible without modifying simulation properties. You can automatically generate relevant OCP properties as interface constraints (instead of assertions to be verified) that ensure verification occurs under proper input requirements.

Users report reduced verification debugging time right from the outset because of the finely-tuned scope of the property sets. If the design specification changes over time, updating the verification environment is a simple matter of re-running the IP Generator on the updated OCP configuration file. Subsequent design family generations with additional functionality no longer need to endure long debugging efforts to repeatedly identify and remove unused property sets. The IP Generator ensures that the verification environment includes only the properties necessary for verification of the specific design implementation.

Summary

OCP is a flexible, synchronous, communications protocol now shipping in excess of one billion units every year. The flexibility creates a great deal of opportunity to customize the protocol to only those specific functions required for a design, but flexibility in implementation generally means complications for verification. Designing a reusable verification environment presents challenges for the developers due to the highly customizable nature of the protocol.

If a team chooses to go with a pre-packaged solution, they must take care to ensure that the verification flow analyzes only the relevant portions of the property sets. This may require some level of protocol expertise to perform efficiently. If the team intends to use formal verification, they must take care to understand which properties are suitable and which they must rewrite. A

better alternative is to leverage Jasper's OCP IP Generator to automatically deduce the required subset of properties specific to the design. The flexibility of the output is readily adaptable to mixed-RTL designs and requires little additional OCP knowledge beyond what is already coded in the design. The OCP IP Generator produces output that is efficiently modeled for formal verification, providing the highest confidence levels possible for the verification environment.

Once the verification team identifies a formal-friendly OCP property solution, they can devise and execute a concrete verification plan. Protocol verification should be thorough, and OCP's configurability can create verification challenges if the team does not plan properly. By generating a hierarchical verification plan that clearly delineates the work to be done, the critical paths to be addressed, and the verification technologies employed, engineers can not only make their verification environments effective, but re-usable. Verification planning tools can greatly ease the amount of work necessary to set up and maintain a verification testplan.

Working Group Updates

Meta Data Working Group:

The Metadata Working Group (MDWG), has released the package of metadata vendor extensions. These extensions are enhancements created to fully capture flexible interfaces (such as OCP) using the IP-XACT format defined by SPIRIT Consortium. The recently released package is both IP-XACT 1.4 and IEEE1685 compatible. The MDWG is also creating OCP configuration and interface compatibility checkers to be released later in the year. For more information on the metadata vendor extension package please see our data sheet available at: <http://www.ocpip.org/datasheets.php>

Specification Working Group:

The Specification Working Group is addressing minor Errata items, performance parameter work, fence and barrier items, while also, prioritizing goals for 2010 as provided by OCP-IP's Technical Vision Working Group.

Functional Verification Working Group:

The Functional Verification WG continues targeting the definition of the functional verification checks and coverage to support OCP 3.0. Current work is focused on Cache Coherence Extensions, specifically targeting configuration checks, signal checks and transaction-level checks.

NoC Benchmarking Working Group:

The NoC BWG has recently completed an update to the Transaction Generator (TG) tool, simplifying installation and ease-of-use while also easing the process of connecting the OCP-IP TLM Modeling Kit TG to various network-on-chips. The Group has also been working on a memory modeling technical article, and hopes to prepare other technical articles regarding the TG during the summer.

Marketing Working Group:

The Marketing Working Group has recently completed presentations at the SystemC and SoC Debug Integration and Applications workshop, which was an ECSI event co-located with DAC. In addition, the OCP-IP System Level Design Working Group gave a presentation at NASCUG and received several mentions of their work in other presentations during the event. Finally, a presentation titled "Maximizing Multichannel DRAM Performance by Invisible Load Balancing" was given at Multicore Expo. As usual, we remain very active helping member companies compose and place their OCP-related articles and conference papers, while publishing the OCP-IP newsletter and regular press releases. If your company would like assistance placing an article, prominently targeted to the industry or directly to our OCP-IP-focused community, please contact admin@ocpip.org.

Debug Working Group:

The Debug Working Group continues to identify required instrumentation signaling extensions and example cases for debug of multi-core systems that support OCP 3.0 cache and power management features. These may include SMP, AMP, multi-threaded, and other system architectures. Preliminary goals are for OCP 3.0 compatible debug systems white papers to be published along with an updated debug specification supporting OCP 3.0 to be available later this year.

Network-on-Chip Activities at KTH

Zhonghai Lu and Axel Jantsch
KTH – Royal Institute of Technology,
Stockholm
<http://www.ict.kth.se/nostrum/>

As a pioneering group, NoC research at KTH started in year 2000. The KTH NoC research has been developed under the name Nostrum, which intends to provide a sustainable technology to address the communication crisis in the nano-regime billion-transistor system-on-chip design.

The Nostrum NoC research has been looking into a number of key issues ranging from NoC architectures to performance analysis, from Quality-of-Service provision to application mapping, from 2D to 3D architectures. Various interesting results have been produced. To mention, just a few snapshots: Nostrum has initially proposed mesh architecture where nodes are organized in a 2D array. Each node hosts one or multiple cores connected to the on-chip network via a router. This simple architecture has become very popular today. The network conducts adaptive deflection routing while guaranteed throughput can still be achieved and formally reasoned. The Nostrum NoC simulator (NNSE) has

enhanced its ad-hoc communication interface to standard AXI interface. Performance analysis has been focused on both worst-case analysis using network calculus and average-case analysis using queuing theory etc.

Over the last ten years, KTH has established itself as one of leading players in the NoC area. Currently the NoC research at KTH has been extended from network centric to system centric, i.e. combining the NoC technology with the many-core technology and distributed memory, investigating both hardware architectures and embedded software, and applying advanced hardware and software technologies to real applications. One example is the architectural support for distributed shared memory, where communication-related functions, like computational functions, are now programmable.

KTH NoC researchers have been strongly supporting the NoC Benchmarking Working Group at OCP-IP from the very beginning. Specifically, they have led in the definition of the Network-on-Chip Benchmarking Specification, Part II, which facilitates researchers to evaluate and compare different NoC platforms.

Si2 News

A lot has been going on recently at Si2. Earlier this year we formed the OpenPDK Coalition, which will define a set of open standards to allow a PDK to be as portable across foundries and as agnostic to EDA tools, as possible. The Si2 OpenPDK will enable greater efficiency in PDK development, verification and delivery, and will provide equivalent support to all foundries, all EDA tool vendors, all IP providers, and all end-users.

In late May, TSMC and its co-development partners Mentor and Synopsys, donated iDRC, a vendor-neutral language for describing IC design rules. iDRC is an open specification that makes it possible for TSMC and its customers to create physical verification design kits that allow easier support of physical verification products from different EDA vendors. iDRC is consistent with the Si2 Design for Manufacturing Coalition's (DFMC) OpenDFM vision, and is a great example of meeting industry challenges with open solutions developed through the collaboration of Si2's member companies.

In June, Si2 announced it's Board of Directors for the 2010-2011 term. They include: AMD – Jim

Miller, vice president of Design Engineering; Apache Design Solutions - Vic Kulkarni, senior vice president and general manager of RTL Business Unit; ARM, Inc. - Dr. John Goodenough, world wide director Design Technology; Cadence Design Systems, Inc. – Dr. Charlie Huang, senior vice president and chief strategy officer; GLOBALFOUNDRIES - Dr. Moji Chian, senior vice president, Design Services and Enablement , IBM – Dr. Leon Stok, vice president, Electronic Design Automation Technologies; Intel Corporation - Rahul Goyal, director, EDA Business; LSI - Prabhakaran (Prabhu) Krishnamurthy, senior director, Design Tools & Methodology; National Semiconductor - James Lin, vice president of Technology Infrastructure; and Synopsys - John Chilton, sr. vice president, Marketing & Strategic Development.

And finally, Steve Schulz, President & CEO of Si2 now has a very popular blog being hosted at Chip Design Magazine. Check it out for commentary on important industry topics: <http://chipdesignmag.com/bayer/>

Recent Publications

Available at <http://www.ocpip.org/articles.php>

Press Releases

May 10, 2010 OCP-IP Delivers IEEE1685 OCP Vendor Extensions

Now Available!

NEW! IEEE 1685 Vendor Extensions

Vendor Extensions provide a way to fully describe configurable interfaces, (such as OCP) in machine-readable XML structure in an IEEE standard format. They are compatible with both IP XACT 1.4 and [IEEE1685](#). The package is available to both OCP-IP members and non-members alike. Members may access the OCP Metadata Vendor Extension package by completing the online click-through [Commercial Metadata Vendor Extension License](#). Non-Members may access the package via online click-through [research license](#).

OCP 3.0 Specification

The Specification Working Group released the OCP 3.0 Specification in November. This latest version contains extensions to support cache coherence and more aggressive power management, as well as an additional high-speed consensus profile and other new elements. For a copy complete our [Research License Agreement](#).

OCP Checker Now Part of CoreCreator II

The OCP checker is a fourth-generation solution for validating protocol compliance of master and slave devices using OCP. It is based on SystemVerilog assertions (SVA) and can be used with all major logic simulators. It supports the complete set of protocol compliance checks defined in the OCP specification and spans the full range of OCP socket configuration options. The OCP checker can also generate trace files in the standard ".ocp" format for post-processing. It can be obtained, as part of CoreCreator II [here](#). For a free copy contact admin@ocpip.org

Debug Specification Version 1.0

The Debug Specification provides guidelines and recommended signal interfaces for on-chip debug of OCP-based systems and related multicore architectures. It describes a debug socket as a framework for IP and tools providers to develop comprehensive and re-usable debug and instrumentation environments that provide on-chip

April 7, 2010 Altera, Digitite, Global Unichip, Innotech, PDTi, and Xtrillion Join OCP-IP

Articles

OCP and Verification of configurable OCP Interfaces - Jasper Design Automation

analysis and control features. These include trace, triggering, multicore synchronization, etc., along with recommendations for integration within ESL environments. For a copy of the spec click [here](#).

NoC Benchmarking Specification, Part 2

Part 2 of the two-part NoC Benchmarking Specification presents a generic NoC architecture, a comprehensive set of synthetic workloads as micro-benchmarks, workload scenarios and evaluation criteria. These micro-benchmarks enable you to measure and pinpoint particular properties of NoC architectures, complementing application benchmarks. For more information, [click here](#).

NoC Benchmarking Specification, Part 1

The specification presents a modeling methodology for applications running on multicore systems and it defines an XML format for documenting and distributing NoC benchmarks. It defines a black-box view of the processing elements that discloses only the relevant computational aspects for interacting with the on-chip data transport mechanism. Download our [NoC white paper](#) for more information

OCP SystemC TLM Kits

The new kit is the first, and most advanced TLM-2.0 based, industry-ready kit in existence today. The kits significantly increase performance, ease of use and ensures alignment with the OSCI 2.0 standard. The kits are free as part of OCP-IP membership. For more information contact admin@ocpip.org

NEW! Transaction Analysis Tool

The Tool is an innovative, detailed OCP transaction viewer that enables fine-grained analysis of bus transactions. A complete transaction sequence can be traced from request to response along with a host of related information about the transaction. For a free copy contact admin@ocpip.org