

OCP-IP News

Partner Update: Silicon Integration Initiative (SI2)

Silicon Integration Initiative (Si2) has recently released important new upgrades for some of its flagship standards. The latest OpenAccess release now includes a multithreading capability, 32nm constraints unique to this particular technology node, as well as other functional enhancements. This first release of multi-threading will support an initial set of use



models at a high-level; the set of use models is expected to be further extended in future releases based upon user experiences and feedback.

OpenAccess will now collaborate with the

application to achieve the best performance for both single-threaded and multi-threaded scenarios. The 32nm Constraint Release includes 19 new constraints that are now natively supported in OpenAccess. These are in addition to over 100 such constraints that support other technology nodes in describing physical layout parameters for such items as minimum spacing, width and enclosure checks. Descriptions and diagrams explaining semantics of the enhancements were also supplied as part of the release. In other news, we are pleased to welcome TSMC to the OpenAccess Coalition. The new version of the Common Power Format (CPF 2.0) includes enhancements and new capabilities in two major categories. Guided by the Si2 Interoperability Guide for Power Format Standards, the release of CPF 2.0

includes the following features to improve interoperability with IEEE 1801-2009: the new concept of generic mode to model either a power mode or a functional mode; the improved hierarchical flow to support output and bi-directional virtual ports; the support of pg_type in supply net connection; more flexibility in modeling different types of isolation, level-shifter and retention logic. In addition, based on contributions from member companies and collaboration with the Low Power Coalition (LPC) Modeling Working Group, the following extensions are included in the CPF 2.0 release: the new concept of power design to further improve hierarchical low-power design flow; the improvements in macro-modeling of mixed-signal IP with low power features; simplified modeling methodology for I/O pads with complex power management logic; added flexibility for control of corruption semantics in power-aware RTL simulation; and extensions to model new low power standard cells such as multi-bit isolation and level-shifter cells, multi-stage level-shifters, and others.

A good summary of all Si2 activities, including milestones met in 2010 as well as plans for 2011 in all 4 major projects (OpenAccess Coalition, OpenPDK Coalition, Design for Manufacturability Coalition, and Low Power Coalition), can be found in the Si2 2010 Member Report, located at: <http://www.si2.org/?page=1310>

President's Overview



Ian Mackintosh
OCP-IP Chairman and President

I would like to open this edition of the OCP-IP Newsletter by offering my heartfelt condolences to our friends and colleagues in Japan for the devastation caused by the recent earthquake and tsunami. We send our best wishes for a full and speedy recovery from the devastation and challenges that lie ahead.

Most economic indicators show some improvement in 2011 over last year. I am very excited for the prospects this improvement brings, not only for OCP-IP, but to the semiconductor industry, as a whole, as we continue work to further streamline operations and bring exciting new products to market. To see just a small sample of the many leading edge products leveraging OCP, please see our newly updated "[OCP Inside Presentation](#)."

As part of the expansion of our infrastructure, the Functional Verification WG has completed targeting the definition of the functional verification checks and coverage to support OCP 3.0. The group has largely completed the work focused on Cache Coherence Extensions, specifically targeting configuration checks, signal checks and transaction-level checks. The final set of verification documents is expected for release in 2Q11.

In addition, the NoC Benchmarking Working Group has released a new white paper titled [OCP-IP Network-on-Chip Benchmarking Work Group Overview](#). For more information on this paper, please see our detailed description on page 7. Also, this Working Group is exploring the opportunity to publish models developed utilizing our Transaction Generator Package. For a copy of the [Transaction](#)

[Generator](#), please [click here](#). Stay tuned for more information on available models in future editions of the newsletter.

Our Marketing Working Group (MWG) has recently completed gathering and posting the [OCP-IP DATE Conference presentations](#) and continues helping member companies compose and place their OCP-related articles and conference papers, and continues publication of the OCP-IP newsletter. They have recently created and published press releases announcing 7 new members to OCP-IP, and other items listed in the box, below.

If your company would like assistance placing an article, prominently targeted to the industry or directly to our OCP-IP-focused community, please contact admin@ocpip.org.

For a full update on the activities of all working groups, please see page 5 of this newsletter.

Sincerely,
Ian R. Mackintosh
Chairman and President, OCP-IP

Recent Press Releases:

March 14, 2011 - [Magillem Platform Assembly solution supports OCP Vendor Extension for IEEE 1685 IP-XACT](#)

March 14, 2011 - [OCP-IP Announces Online DATE Virtual-Conference Presentations](#)

February 28, 2011 - [Cadence Opens and Extends Verification IP Catalog for Use Across Silicon, SoC and System Development](#)

Facing up to the challenges of SoC integration

Courtesy Chip Design Magazine



The challenge around IP integration has become pivotal in determining whether design teams of advanced system on chips (SoCs) meet their time-to-market and performance goals. The rapid growth in the number of available intellectual property (IP)

blocks has both enabled and paralleled the increase in the size and complexity of SoCs. Semico Research Corp. reports that current SoC designs now average more than 50 IP blocks, and that number is forecast to double by 2014. There has been similar growth in the number of interface IP blocks being integrated into SoCs, including: high speed, such as PCI Express®, Ethernet and USB 3.0; low speed, such as I2C, GPIO and SPI; and application specific, such as HDMI and MIPI. At the same time, the complexity of these protocols and resulting interoperability issues are rapidly increasing due to the consumer's voracious appetite for more speed and features.

The number of diverse IP solutions coupled with the complexity of the protocols underscores the need for easy-to-configure, easy-to-use, high-performance verification IP, which helps engineers get up-to-speed on new protocols and quickly debug protocol-related issues. However, verification engineers are not necessarily protocol experts. Instead, they are verification experts who try to confirm that all of the IP has been successfully integrated into the system. As a result, these engineers rely on verification IP to encompass the various protocol requirements and standards.

Today, SoC developers see little reason to develop highly complex interface IP blocks because this requires very precise domain expertise, gives little opportunity to differentiate their end-products and increases time to market. Consequently, the value of IP providers lies in delivering a high-quality product that designers can drop into their design with a high level of trust. Extensive verification is still needed, but the focus is now on integration testing, rather than compliance testing. Re-verifying compliance of an IP block after integration is redundant and a waste of valuable resources and time. It also requires a great deal of expertise to interpret results and reach sufficient coverage. This is why it's

important to pick a tried and trusted IP provider at the outset..

There is a great deal of burden placed on IP developers to not only verify the compliance of the external protocol, but to also ensure that their IP plugs into the system buses. One of the big problems in integrating IP from multiple internal and external vendors is resolving the interoperability issues. This is mitigated through the use of standards, like the ARM® AMBA® interconnect, based around the use of ARM processors; industry standards like Open-Core Protocol (OCP); and internal buses that are shared within and across companies to foster IP sharing. Nevertheless, this remains one of the problem areas of system integration. With so many IP blocks being brought together, small differences in the interpretation of the specifications can lead to major integration problems.

The focus for the system integrator has consequently shifted from compliance testing to system-oriented verification. The main issues they face are: how to verify that multiple IP blocks are working in the larger system, how to stress those interfaces in the context of the larger design and how to quickly debug problems at the interfaces of the SoC.

A technique that SoC designers use, (as reported by Semico Research), is to build the most complex family member of a design first and then create derivatives by removing features and functions. This technique is used with the intent to reduce cost and time-to-market. With the globalization of engineering resources, and as companies create alliances to share the cost of creating a new platform, it is reasonable to expect that some of these derivatives may be created by remote groups, or by groups in partner corporate entities which have different environments. This increases the need for testbench reuse and portability, as well as that for verification IP which is both simple to reconfigure and use. There is no guarantee that any new team has the protocol or verification IP expertise for all of the interfaces in the derivative design.

Verification IP should consequently be made accessible to more than protocol and methodology experts. Verification IP needs to include features which make it easy for verification engineers to quickly ramp-up on new protocols, integrate them into their environments, interpret the protocol activity

OCP-IP DATE Conference Presentations Now Available!

on the interface, debug issues, know the status of coverage and deliver high-performance integration. In short, the system integrator needs access to a wide range of verification IP, and must be able to quickly and easily integrate these into their testbench to verify system integration.

This can be a big challenge with verification IP solutions which are based upon support for specific methodologies or simulators. SystemVerilog and methodologies like UVM and VMM improve interoperability of verification IP and make it simpler for engineers to ramp-up on new offerings from multiple vendors. These tools not only make it easier to integrate the verification IP through the use of a consistent methodology and interface, but also provide the benefits of common debug applications and higher performance from running natively in the simulator engines. SystemVerilog also gives greater visibility into the layers of the protocol, extending the ability to add application-specific coverage points and functionality, and perhaps even opportunities to browse through the source code of the verification IP using debug tools.

One of the big opportunities for verification IP providers is to help verification engineers determine the optimum coverage really needed to complete integration testing. There is often a gray area that can fall between a couple of simple reads and writes, and full compliance testing. Engineers tend to err on the side of over-testing and frequently use the full coverage of the protocol to test integration. This creates lots of additional and unnecessary work, supplemental to the set of tests really needed to verify that a core is soundly integrated into the SoC. It falls upon the experts who develop verification IP to provide guidance on when integration testing can be considered complete.

With language and methodology convergence, there are many more opportunities for verification IP developers to create new features and new levels of productivity, thereby assisting verification engineers with protocol-based verification. This is a good thing, because with SoC complexity growing at a fast pace, innovation around commercial IP verification needs to also keep accelerating.

Neill Mullinger is a group marketing manager at Synopsys. In this role he focuses on verification IP and methodology support and has product manager responsibility for Synopsys Verification IP. Neill joined Synopsys in 2000 and has over 20 years experience in the hardware and EDA industries, bringing an extensive background of verification experience to bear on product and methodology definition.

Open Core Protocol International Partnership has once again posted their annual online "Presentations from DATE". The Design Automation and Test Europe (DATE) Conference is held 14-18 March 2011 in Grenoble, France. These presentations offer a fresh opportunity to see the latest products, tools, and services utilizing OCP technology.

Presentations are freely available and discuss the diverse issues, challenges, and topics surrounding re-usable IP, including: IP development, purchasing, interconnect, verification and testing, IP quality, and network on chip (NOC) from OCP-IP member companies: Alpha Data, Carbon Design Systems, Cadence Design Systems, CAST, Duolog Technologies, Jasper Design Automation, OCP-IP's NoC Benchmarking Working Group, Sonics, Synopsys, and more.

To review the presentations, please see: http://www.ocpip.org/papers_and_presentations.php

New Member Spotlight

Renesas Corp - Renesas Electronics Corporation (TSE: 6723), the world's number one supplier of microcontrollers, is a premier supplier of advanced semiconductor solutions including microcontrollers, SoC solutions and a broad-range of analog and power devices.



Headquartered in Japan, Renesas Electronics has subsidiaries in 20 countries worldwide. More information can be found at www.renesas.com.

Working Group Updates

Debug Working Group:

The Debug Working Group is actively disseminating the standard framework at conferences and is open for calls to collaborate on a standard debug block at either an ESL or RTL level.

Planned additions to the debug interface 3.0 are cache coherence and power management features for SMP, AMP, multi-threaded, and other system architectures. Preliminary goals are for OCP 3.0 compatible debug systems white papers to be published along with an updated debug specification supporting OCP 3.0 to be available in 1H11. The Debug Group is also developing a work plan for 2011 for approval by the Technical Vision Working Group

Metadata Working Group:

The Metadata Working Group (MDWG), has released a package of metadata vendor extensions in 2010. These extensions are enhancements created to fully capture configurable interfaces (such as OCP) using the IP-XACT format defined by the Accellera Consortium.

The package is both IPXACT 1.4 and IEEE1685 compatible and has configuration checkers for OCP2.2. The MDWG continues to develop the OCP3.0 package which includes bus definition, abstraction definition & configuration checkers for OCP3.0. This package will be released in 1H11. For more information on the metadata vendor extension package please see our data sheet available at:

www.ocpip.org/datasheets.php

System Level Design Working Group:

Since the successful release of the SDL Working Group's Virtual platform (VP), the platform has been updated for compatibility with the most recent release of the core ISS.

The VP is a loosely-timed model of a simple embedded platform which runs the Linux operating system. Some of the memory-mapped peripherals are modeled using the OCP Modeling Kit ("OMK") which demonstrates the use of the kit. To obtain an overview and basic understanding of the Virtual Platform, please refer to our [Datasheet](#). To download a copy of the VP, click [here](#).

The SLD WG is also nearing the release of adapters which allow efficient connection between several levels of abstraction using the new OMK.

Specification Working Group:

The Specification Working Group is continuing work on OCP 3.1, which will include extensions in the area of memory semantics to support weakly ordered memory systems and in the area of performance parameters that describe available IP-core concurrency which helps system integrators optimize performance while minimizing hardware costs.

NoC Benchmarking Working:

The NoC BWG recently published a white paper titled [OCP-IP Network-on-Chip Benchmarking Work Group Overview](#). This paper presents a summary of the work and total infrastructure developed and provided by the workgroup, including tool releases, specifications, and other important white papers and technical articles.

Functional Verification Working Group:

The Functional Verification WG has completed targeting the definition of the functional verification checks and coverage to support OCP 3.0. They have largely completed the work focused on Cache Coherence Extensions, specifically targeting configuration checks, signal checks and transaction-level checks. The final set of verification documents is expected to be released in 1H2011.

Marketing Working Group

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With the move to manycore systems having hundreds of cores on a single die, the network-on-chip (NoC) used for intra-chip communication will have a direct impact on the overall system performance and power. There has been a large body of work exploring various network architectures in the past few years. However, most of these works use synthetic benchmarks and/or are focused on choosing network architectures at design time. Given that these manycore systems will be



used in a variety of computing domains ranging from data centers to embedded systems, the workloads

running on these systems will vary significantly. It is, therefore, imperative to investigate run-time management techniques that will adapt the NoC architecture to the workload running on the manycore system.

The focus of our ongoing project at Boston University is to develop run-time NoC management techniques that jointly optimize for energy and performance of the entire manycore system under a variety of workloads. We are exploring run-time changes to network topologies, router architectures and channel architectures to identify an optimal network architecture that suits the current workload. We have interfaced Booksim (a network simulator developed at Stanford University) with M5 (a system simulator developed at University of Michigan) to develop a realistic and cycle-accurate evaluation platform.

As a first case study, we have evaluated the impact of change in the channel width for a bus and crossbar topology. For our analysis, we considered a 64-core system with a private L1 cache. We considered a shared memory programming model, and explored distributed and private L2 cache architectures. We selected parallel applications from the PARSEC

and NAS benchmark suite, both of which have been widely used in parallel system studies.

The proposed reconfiguration policy uses the energy-delay product (EDP) to choose the network channel width. As the workload instructions per cycle (IPC) closely tracks the system energy-delay product (EDP), we use regression models to predict the IPC, which is used to appropriately scale the channel width. The experimental results show that in systems with private and distributed L2 caches our policy reduces EDP by 49.3% and 23.9%, and 65.5% and 20.6% on average with bus and crossbar, respectively, in comparison to statically setting the channel width (*). Moving forward we plan to explore other run-time changes to the network architecture, including network topologies, router architectures and channel architectures.

* More details can be found in our paper published in GLSVLSI 2011



Ajay Joshi joined the ECE department at Boston University as an Assistant Professor in Fall 2009. Prior to joining Boston University, Ajay Joshi received Ph.D. from the ECE department at Georgia Tech as part of the

Advanced Interconnect Modeling and Design Group led by Prof. Jeffrey Davis, and then worked as a postdoctoral researcher in the EECS department at MIT as part of the Integrated Systems Group led by Prof. Vladimir Stojanovic. His research interests span across various aspects of VLSI design, including circuits and systems for communication and computation, and emerging device technologies including silicon photonics and carbon nanotubes.

Partner News From ECSI

This year's DATE conference in Grenoble, France, focused on embedded systems and the increase in software complexity due to the growing number of cores in today's embedded systems and the practice of loading third party applications onto embedded devices. S4D (System, Software, SoC and Silicon Debug) workshop organized by ECSI on the Monday just prior to DATE, also focused on this topic. Experts from different areas presented and discussed embedded system debugging and test requirements and solutions. Presentations from tool vendors, processor providers and researchers looked at debugging challenges from different perspectives.

Albrecht Mayer from Infineon, presented Automotive challenges of on-chip debugging, dealing with filtering trace data for multi-core applications. Compared to consumer markets, the automotive industry has moderate time-to-market challenges and software complexity. Stephane Marmey from ST's TV processor division and Sudharsan Srinivasan from Nokia, both reported a huge increase in software complexity over the last two years. To improve time-to-market, ST made their GDB based software debugger available for RTL simulations, making early software development and debugging possible before silicon is available. They used Cadence ISX to bridge debugger availability on RTL processor models when moving from fast CPU models to debugging on the target with high accuracy as early as possible. Early availability of models for software debugging at high speed and with highest accuracy, was presented by Bill Neifert from Carbon, a supplier of Virtual Prototype Systems. Carlo del Giglio from Jasper presented a technology to find the root cause of bugs faster using formal methods for post-silicon debugging. The usual problem of formal methods related to state explosion was avoided by focusing on identifying the root cause of one bug, instead of proving the correctness of a whole design. Another type of bugs, thermal anomalies in packed ICs caused by shortcuts, were presented by Antoine Reverdy, Sector Technologies.

Francois Cerisier, EASii-IC, gave an overview on how to automate debugging and hardware/software co-debugging with tools from different

Pad Brouillette, Chair of S4D Conference (October 5-6, 2011), in Munich highlighted the growing complexity of today's electronic systems and presented Intel's trace-based debugging solution to improve hardware/software integration time.

A lively discussion and demos of debugging tools concluded an intense day on one of the most challenging topics for today's system developers. If you want to join the discussion or present your view and solution, submit a proposal for the S4D conference at <http://www.ecsi.org/s4d>.

New NoC WG Overview White Paper Available!

OCP-IP's NoC Benchmarking Working Group recently published a white paper titled "[OCP-IP Network-on-Chip Benchmarking Work Group Overview](#)."

This paper presents a summary of the work and total infrastructure developed and provided by the OCP-IP Network-on-Chip benchmarking workgroup, including tool releases, specifications, and other important white papers and technical articles.

The Network on Chip Benchmarking Working Group has also issued an open call for Benchmarks to be distributed to researchers. NoC researchers may submit benchmarks from any application domain to be included. For more information on the call for benchmarks, please see http://www.ocpip.org/ocpspec_call_for_benchmarks.php

To download a copy of the Overview White Paper click [here](#).

Now Available!

NEW! OCP Virtual Platform (VP)

The VP is a loosely-timed model of a simple embedded platform which runs the Linux operating system. Some of the memory-mapped peripherals are modeled using the OCP Modeling Kit (OMK), demonstrating the use of the kit. To obtain an overview and basic understanding of the Virtual Platform, please refer to our [Datashheet](#). To download a free copy of the VP, click [here](#).

NEW! Transaction Generator

The Transaction Generator (TG), is a transaction level (TL) SystemC simulator for benchmarking network-on-chips (NoCs) used in multiprocessor system-on-chip (SoC) applications. Utilizing this tool makes simulation of larger systems substantially faster and the results obtained at this higher level can be accurately used as an initial estimate in selecting and fine-tuning NoCs. The tool is freely available through GNU LGPL. For your copy click [here](#)

NEW! OCP Tracker

Is a software tool that provides graphical performance, statistical and transaction analysis of OCP interfaces and fabrics. It also enables validation of performance metrics via a built-in regression manager. OCP-Tracker seamlessly interfaces with OCP-IP's [CoreCreator II](#) trace files to allow bandwidth, latency and other types of performance metrics to be analyzed. To request your copy of Tracker click [here](#).

IEEE 1685 Vendor Extensions

Vendor Extensions provide a way to fully describe configurable interfaces, (such as OCP) in machine-readable XML structure in an IEEE standard format. They are compatible with both IP XACT 1.4 and [IEEE1685](#). The package is available to both OCP-IP members and non-members alike. Members may access the OCP Metadata Vendor Extension package by completing the online click-through [Commercial Metadata Vendor Extension License](#). Non-Members may access the package via online click-through [research license](#).

OCP 3.0 Specification

The Specification Working Group formally released the OCP 3.0 Specification in November, 2009. This latest version contains extensions to support cache coherence and more aggressive power management, as well as an additional high-speed consensus profile and other new elements. For a copy complete our [Research License Agreement](#).

OCP Checker Now Part of CoreCreator II

The OCP checker is a fourth-generation solution for validating protocol compliance of master and slave devices using OCP. It is based on SystemVerilog assertions (SVA) and can be used with all major logic simulators. It supports the complete set of protocol compliance checks defined in the OCP specification and spans the full range of OCP socket configuration options. The OCP checker can also generate trace files in the standard ".ocp" format for post-processing. It can be obtained, as part of CoreCreator II [here](#). For a free copy members can contact admin@ocpip.org

Debug Specification Version 1.0

The specification provides guidelines and recommended signal interfaces for on-chip debug of OCP-based systems and related multicore architectures. It describes a debug socket as a framework for IP and tools providers to develop comprehensive and re-usable debug and instrumentation environments that provide on-chip analysis and control features. These include trace, triggering, multicore synchronization, etc., along with recommendations for integration within ESL environments. For a copy of the spec click [here](#).

NoC Benchmarking Specification, Part 2 of 2

The specification presents a generic NoC architecture, a comprehensive set of synthetic workloads as micro-benchmarks, workload scenarios and evaluation criteria. These micro-benchmarks enable you to measure and pinpoint particular properties of NoC architectures, complementing application benchmarks. Click [here](#) for a copy of the spec.

NoC Benchmarking Specification, Part 1 of 2

The specification presents a modeling methodology for applications running on multicore systems and it defines an XML format for documenting and distributing NoC benchmarks. It defines a black-box view of the processing elements that discloses only the relevant computational aspects for interacting with the on-chip data transport mechanism. Click [here](#) for a copy of the spec.

OCP SystemC TLM Kits

The new kit is the first, and most advanced TLM-2-based, industry-ready kit in existence today. The kits significantly increase performance, ease-of-use and ensure alignment with the OSCI 2.0.1 standard. Kits are free as part of OCP-IP membership. Non-Members may obtain a free research version. For more information contact admin@ocpip.org

Transaction Analysis Tool

The OCP Conductor Tool is an innovative, detailed OCP transaction viewer that enables fine-grained analysis of bus transactions. A complete transaction sequence can be traced from request to response along with a host of related information about the transaction. For a free copy contact admin@ocpip.org