

OCP-IP News

Partner Update: EDAC and CELUG conduct Enterprise Licensing and EDA/HPC IT Event at DAC 2011 in San Diego.



On June 8 and 9, the EDA Consortium (EDAC) and the Centralized Enterprise Licensing Users Group (CELUG), conducted

the Enterprise Licensing and EDA/HPC IT meeting in San Diego, CA. This event was co-located with the Design Automation Conference (DAC).

The two day event consisted of a day of presentations related to enterprise software licensing, followed by a day of EDA High Performance Computing (EDA/HPC) presentations. This event also provided valuable networking opportunities which will help address current problems and provide a network of support for future issues that can arise throughout the year.

The enterprise software licensing day began with an update on status and plans from Flexera, a key provider of licensing solutions for the EDA market. That was followed by a presentation by the EDA Consortium Anti-Piracy committee, which addresses piracy issues of common concern to EDAC members. Following that, five major EDA software vendors presented their roadmaps and “best practices” recommendations. This included presentations from Agilent, ANSYS, Cadence Design Systems, Mentor Graphics, and Synopsys. Rounding out the enterprise licensing day were presentations from

licensing reporting providers License Tracker, OpenIT, Runtime Design Automation, and TeamEDA.

EDA and HPC IT presentations filled the second day of the meeting. The day opened with HPC/Grid cloud computing presentations from Platform Computing and Univa. The EDAC Interoperability (OS Roadmap) Committee presented the current EDA industry roadmap, while Red Hat and Oracle presented their roadmaps for RHEL and OEL, respectively. The working lunch included a presentation on the cloud offering from Synopsys.

This busy second day continued with EDA infrastructure presentations from Dell, HP, Isilon, NetApp, and Panasas. Processor vendors AMD and Intel included status and roadmap presentations. Rounding out day two was a presentation from HPC system integrator ASG.

Although previously held in conjunction with Flexera’s SoftSummit meeting, CELUG teamed up with EDAC to hold the 2011 event at DAC, the premiere conference and trade show for the EDA industry. Attendance at this event included more than 65 attendees from around the world. In addition to the presenters, attendees included licensing managers and administrators who maintain, update and report utilization and forecasting metrics on use of software tools, as well as IT managers and administrators, who maintain and support compute and data intensive EDA/HPC Grids.

President's Overview



Ian Mackintosh
OCP-IP Chairman and President

Welcome to this edition of the OCP-IP newsletter. I recently returned from DAC where I had the pleasure of meeting with many members of OCP-IP. Most of my discussions suggest that the industry will be taking an optimistic but cautious approach to the remainder of 2011.

Our goal at OCP-IP has always been to create an organization with the tools and structure necessary for our members to quickly and easily leverage the benefits of the OCP specification in their designs. Naturally, a paper standard without an infrastructure and tool support is less attractive to use.

To enhance the value of our members' use of the OCP TLM kit, we recently announced the availability of a NEW relaxed commercial version of our TLM License. This new license allows OCP-IP members to modify or create derivative works.

In addition, the new license distinguishes between source and binary code redistribution and provides a clear definition for derivative work. It now also permits uses outside of semiconductor products such as research, training, in products like virtual platforms, consultancy reports or for EDA tool testing. Distribution to software customers is now allowed for OCP-based product development. Finally, the new license removes auto-termination conditions ensuring Member companies no longer risk violating the agreement through oversight. Members interested in reviewing copies of the new commercial TLM license agreement should contact admin@ocpip.org

OCP-IP has also added an Accurate Dynamic Random-Access Memory Model (ADM) package to our deliverables. A demonstration program

provided in the package can be used to test the delay and throughput of the DRAM for certain traffic flows, more accurately representing the performance of systems and enabling a realistic evaluation of Networks on Chip (NOCs) deployed in those systems. For more information on the ADM, please see page 7.

We are proud to announce that our latest comprehensive set of Functional Checks and Assertions from the Functional verification working group is already available to Sponsor-Level Members for review and comment. For a copy of the latest Functional Checks and assertions please contact admin@ocpip.org

Lastly, our marketing working group has updated our "OCP-Inside" presentation. To see just a small sample of the many leading edge products featuring OCP, please see our newly updated "[OCP Inside Presentation.](#)"

For a full update on the activities of all working groups, please see page 5 of this newsletter.

Recent Press Releases:

June 07, 2011 - [OCP-IP Delivers New Accurate DRAM Memory Model Package](#)

May 24, 2011 - [OCP-IP Develops New Relaxed Commercial Use License For SystemC Transaction Level Modeling Kit](#)

May 17, 2011 - [OCP-IP Announces Updated Functional Checks and Assertions Available to Sponsor-Level Members](#)

Creating A SoC Virtual Platform For Embedded Software Development

Umesh Sisodia, Girish Verma, Ashwani Singh, Dheeraj Kaushik: CircuitSutra Technologies

Courtesy Electronic Design Magazine

Today's system-on-chip (SoC) designs incorporate various input-output capabilities and are multi-core systems with fast communication protocols. SoCs often incorporate various processing elements for multimedia and networking applications. The convergence of computing, communications, and multimedia data processing onto one chip pushes SoC complexity in two areas: SoC integration and software development.

No company today designs the complete SoC itself; they source the complement of IP cores from different vendors. Integrating IP from different vendors in a single SoC and making them interoperate is a highly complex task. The IP vendors are under pressure to support all the popular interfaces and make their IP suitable for a wide range of customers. To address SoC integration issues, the industry has been moving toward standardizing the IP core interfaces to achieve high reuse. The [Open Core Protocol-International Partnership \(OCP-IP\)](#) is a standards forum focusing on SoC integration concerns. OCP-IP defines a high-performance, SoC, bus-independent interface between IP cores. This makes the IP core independent of the architecture and design of systems in which they are used.

SoC developers not only need to achieve high performance, but the product also must be flexible and programmable. As a result, SoCs are becoming software intensive. Software content on these SoCs comprises low-level firmware, device drivers, telecom/communication stacks, operating system (OS) code, and application software, etc. Development and validation of so much software is a big challenge.

To address these software development challenges, the industry has been adopting more abstract simulation models, which can deliver enough performance and accuracy to enable the software development to begin in parallel with chip development. In this phase, software developer goes through multiple build/execute/debug cycles and overall productivity depends on the simulation speed and ease of debug. [The Open SystemC](#)

[Initiative \(OSCI\)](#) is a standards forum focusing on defining the standards for creating software models of SoC. SystemC is a standard language for modeling of SoC. [OSCI TLM2.0](#) is a standard library for transaction-level modeling. OCP-IP has created an advanced modeling kit by extending OSCI TLM2.0 for the Open core protocol.

The OSCI and OCP-IP standards have the potential to address most of the challenges in current SoC designs. We at CircuitSutra have demonstrated the virtual platform by using the modeling standards from OCP-IP and OSCI. A [demo virtual platform is available for free download](#) from the OCP-IP website.

Using the virtual platform for embedded software development instead of an FPGA board can provide several advantages. It allows hardware design and embedded software development to proceed in parallel, hence reducing the time to market for electronics product. It also provides more powerful debug features needed to develop and verify complex software for a multicore SoC. This article discusses how to create an SoC virtual platform for embedded software development.

It is critical to choose the correct abstraction level when creating an SoC virtual platform. The abstraction level defines how much timing accuracy you will see in simulation as well as the functional accuracy of the hardware models. Which level is right for you? It depends on your purposes for using the virtual platform. These might include embedded software development, RTL verification, architectural exploration, and performance optimization. We will limit discussion to embedded software development, which requires use of the virtual platforms at very high abstraction levels. [Various abstraction levels](#) [FIGURE 1]

For the complete article (including figures) please see the link below to Electronic Design Magazine.

Link: <http://electronicdesign.com/article/eda/Creating-An-SoC-Virtual-Platform-For-Embedded-Software-Development.aspx>¹¹

Working Group Updates

Debug Working Group:

The Debug Working Group is actively disseminating the standard framework at conferences and is open for calls to collaborate on a standard debug block at either an ESL or RTL level. The Group is actively working on additions to the debug interface 3.0 including cache coherence and power management features for SMP, AMP, multi-threaded, and other system architectures. The Group has set a goal for an OCP 3.0 compatible debug systems white paper to be published along with an updated debug specification supporting OCP 3.0 to be available by EOY 2011

Metadata Working Group:

The Metadata Working Group (MDWG), has released a package of metadata vendor extensions in 2010. These extensions are enhancements created to fully capture configurable interfaces (such as OCP) using the IP-XACT format defined by the Accellera Consortium. The package is both IPXACT 1.4 and IEEE1685 compatible and has configuration checkers for OCP2.2. The MDWG continues to develop the OCP3.0 package which includes bus definition, abstraction definition & configuration checkers for OCP3.0. This package will be released in 2H11. For more information on the metadata vendor extension package please see our data sheet available at: www.ocpip.org/datasheets.php

System Level Design Working Group:

The SLD Working Group maintains three download packages: the base OCP Modeling Kit (OMK), the extension package for the OMK (including monitor and abstraction-level-adaptor components), and the example virtual platform (VP) which demonstrates use of the OMK. A new release of the OMK and monitor package is currently being prepared which expands coverage to more of the OCP protocol, adds more adapters, and corrects a few issues discovered by users. The new adapters are native TLM-2.0 and enable efficient connection of loosely-timed, approximately-timed, cycle-accurate and RTL models. Subsequent work in the SLD Working Group will ensure the compatibility of the OMK with the latest versions of SystemC and TLM-2.0 available from OSCI and the major EDA vendors, and collaboration with the Metadata Working Group on use of IP-XACT to automate system-level-design activity with OCP components.

Specification Working Group:

The Specification Working Group is continuing work on OCP 3.1, which will include extensions in the area of memory semantics to support weakly ordered memory systems and in the area of performance parameters that describe available IP core concurrency which in turn helps system integrators optimize performance while minimizing hardware costs.

NoC Benchmarking Working:

The NoC Benchmarking Working Group has recently released an Accurate Dynamic Random-Access Memory Model (ADM) package. The ADM is a configurable, transaction-level model for Dynamic Random-Access Memories (DRAMs). The model package was developed in SystemC using OCP-IP's TLM Kit, and can be combined with other OCP-compatible modules through a OCP TL1 interface. The memory model package was developed based on a white paper focused on the subject of memory modeling titled, "[A Memory Subsystem Model for Evaluating Network-on-Chip Performance.](#)"

The package is freely available to both OCP-IP members and non-members alike, through GNU LGPL licensing at http://www.ocpip.org/memory_model.php.

Functional Verification Working Group:

The Functional Verification WG has completed targeting the definition of the functional verification checks and coverage to support OCP 3.0. They have largely completed the work focused on Cache Coherence Extensions, specifically targeting configuration checks, signal checks and transaction-level checks. The final set of verification documents is expected to be released in 2H2011.

Marketing Working Group

The Marketing Working Group has recently completed gathering and posting several OCP presentation given at DAC and has also updated the "OCP Inside" presentation. In addition, the group continues helping member companies compose and place their OCP-related articles and conference papers, while supporting the ongoing publication of the OCP-IP newsletter and our various press releases.



Dynamic Random Access (DRAM) memory subsystem is a crucial component of a computing system architecture. The system performance largely relies on efficient memory accesses, and design decisions for the system architecture based on trustable memory models. However, current

memory models used in system modeling and performance evaluation are far too simple. They respond to memory access requests either immediately, or with just a fixed delay. As a consequence, such oversimplistic models may mislead the design space exploration of system architectures. Over-optimistic performance data may be generated or wrong performance bottlenecks identified, leading to forced system re-architecting when realistic memory models are in place. Nevertheless, building accurate DRAM models are nontrivial, due to generations of a large variety of DRAM products having a wide range of timing-related constraints.

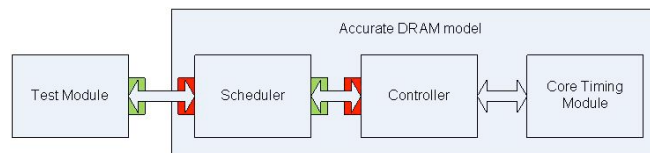
At the Network-on-Chip Benchmarking Working Group (NoC-BWG) of OCP-IP, we have launched efforts to target this challenge. The first effort is to define an accurate DRAM model specification [1], which captures the key timing and access dependency parameters at the lowest level while, at the same time, keeping the abstraction level high enough to make the system development easy. The values of these parameters can be found in either the JEDEC (Joint Electron Device Engineering Council) specification [2] or the DDR model specification (for example, the Micron DDR model [3]). Based on these values, the memory model can produce transaction and history-specific latencies.

Based on [1], the NoC-BWG started the second effort, which is to design and implement an accurate high-level DRAM model in SystemC [4]. A design project was defined by myself and launched at KTH. A team of 4 Masters students, Nan Li, Yi Wang, Huisheng Zhou and Lei Liang, worked on this project under my supervision. The outcome of this project resulted in the release of the ADM (Accurate DRAM Model in SystemC) package.

Figure 1. shows an overview of the ADM package. The accurate DRAM model consists of three major modules: a scheduler, a controller, and a core DRAM timing module.

It is the core timing module which takes into account the major delay parameters of a real DRAM, and imitates its

timing behavior and access dependencies. The scheduler studies the impact of different scheduling policies, such as FIFO, round robin and priority, upon the memory access performance. These scheduling policies can be seen as



examples, and users may design more advanced scheduling policies of their own within the structure. The controller is an interface between the scheduler and the core DRAM timing module. It is possible to combine the scheduler and the controller. However, the separation makes it easier to develop different scheduling functions that may be desired by users.

As also shown in Figure 1, there is a test module provided in the ADM package. The test module generates transactions to test the DRAM performance while under test. It also functions as an example for how to hook user-designed modules into the accurate DRAM model. A demo program provided in the package can be used to test the delay and throughput of the DRAM for certain traffic flows.

The ADM provides a configurable, cycle-approximate, transaction level timing model for realistic DRAMs.

- Configurable

This means that the user can set different values for the parameters in order to mimic the timing behavior of different DRAMs. One can even configure the simple DRAM models (immediate or fixed-delay response) through the configuration.

- Cycle approximate

For the scheduler and controller, the operations are cycle accurate, but for the DRAM timing model, it is cycle-approximate. As the latencies of DRAMs are expressed in nanoseconds, a higher DRAM speed means a larger approximated number of cycles. According to a given speed of the DRAM, a different number of cycles in delay is to be simulated.

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- Transaction-level

The model is written in SystemC using the OCP TLM Kit. Functions are implemented as function calls.

- Integration friendly

The user can directly use or extend the scheduling function. The model can be combined with other OCP-compatible modules through an OCP TL1 interface. One can integrate one's own traffic generators and interconnect modules to the ADM.

The current ADM uses the following modeling packages: SystemC 2.2.0, TLM 2.0.1, and OCP TLM Kit 2.2x2.1. It has been tested under different platforms: 32-bit Linux Ubuntu 10.04 with gcc 4.4.3, 32-bit Linux Ubuntu 9.10 with gcc 4.4.1, 32-bit Windows XP Cygwin with gcc 4.3.4, and 64-bit Windows 7 Cygwin with gcc 4.3.4. For technical details of the design and implementation of the ADM, please refer to [4].

References:

[1] Krishnan Srinivasan and Erno Salminen. "A memory subsystem model for evaluating network-on-chip performance", OCP-IP white paper, September 2010.

[2] Joint Electron Device Engineering Council, JEDEC Specification, www.jedec.com

[3] Micron Technology Inc., Micron DDR2 specification, <http://download.micron.com/pdf/datasheets/dram/ddr2/256MbDDR2.pdf>

[4] Nan Li, Yi Wang, Huisheng Zhou and Lei Liang. "Design and Implementation of an Accurate Memory Subsystem Model in SystemC", Technical report, KTH. December 2010. (Available in the ADM package.)



Zhonghai Lu is currently an associate professor directing the Dependable Autonomous Systems group at the Department of Electronic Systems, School of Information and Communication Technology at the Royal Institute of Technology, KTH.

New Accurate DRAM Memory Model Package Available!

OCP-IP's NoC Benchmarking Working Group announced the availability of an Accurate Dynamic Random-Access Memory Model (ADM) package. The ADM is a configurable, transaction-level model for Dynamic Random-Access Memories (DRAMs). This model is more accurate than current DRAM models used for system-simulation because it considers the major delay parameters of real DRAMs and imitates their timing behavior with access dependencies captured. A demonstration program provided in the package can be used to test the delay and throughput of the DRAM for certain traffic flows, more accurately representing the performance of systems and enabling a realistic evaluation of Networks on Chip (NOCs) deployed in those systems.

The model package was developed in SystemC using OCP-IP's TLM Kit, and can be combined with other OCP-compatible modules through an OCP TL1 interface.

The package is freely available to both OCP-IP members and non-members alike, through GNU LGPL licensing at http://www.ocpip.org/memory_model.php.

The Network on Chip Benchmarking Working Group has also issued an open call for Benchmarks to be distributed to researchers. NoC researchers may submit benchmarks from any application domain to be included. For more information on the call for benchmarks, please see http://www.ocpip.org/ocpspec_call_for_benchmarks.php

Partner Update : ECSI ESLSyn Conference at DAC

ESLSyn 2011: The first ECSI International Symposium on Electronic System Level Synthesis in cooperation with the IEEE Council on Electronic Design Automation (IEEE CEDA) was held on June 5 and 6, 2011 at the San Diego Convention center. The symposium was organized by ECSI with Daniel Gajski (UC Irvine, USA), and Adam Moraweic (ECSI, France) as general chairs. The technical program committee was chaired by Phillip Coussy (Univ. of Bretagne-Sud, France), and Sandeep Shukla (Virginia Tech, USA).

13 papers were selected for presentation at the conference. The presentations were divided into topics including Co-design, FPGAs and Synthesis, Modeling, and System Design. In addition to the presentation of these regular papers, there were 4 keynote speeches, as well as, an invited presentation by Prof. Daniel Gajski entitled, "Quo Vadis ESL Synthesis?", which led to very interesting debates and discussions.

Dr. Rishiyur S. Nikhil, CTO of Bluespec, Inc. opened the conference with a keynote titled "Rethinking your Assumptions in ESL Design" making a very strong case for not using C/C++ like imperative languages, but as an ESL language. The second keynote, presented by Michael McNamara of Cadence Design Systems, discussed the co-dependent relationship of high-level synthesis and verification, elaborating on ECO management and incremental synthesis technologies.

The second day of the conference was opened with a keynote by Andres Takach, chief Scientist of Mentor Graphics, who outlined ESL model refinement challenges, with particular emphasis on C/C++ based ESL. The final keynote speech discussed the synthesis of distributed real-time embedded software with specific connection to PTIDES project and was given by Prof. Edward Lee, distinguished professor at the University of California at Berkeley.

A panel discussion led by Prof. Sandeep Shukla of Virginia Tech, entitled "ESL Synthesis? Get Real!!!!", concluded that ESL synthesis is very important for the near future, but what we have now is high-level synthesis of individual components and not system synthesis. More research is needed for system synthesis to become a reality. The panelists included Stephen Neuendorffer from Xilinx, Kim Gruettner from OFFIS, Benjamin Carrion Schafer from NEC Corp., and Johannes Stahl from Synopsys.

Xilinx, Cadence, and Mentor Graphics provided tool demonstrations regarding EDA synthesis solutions that provided event participants good insight into the state-of-the-art solutions now available for industrial deployment and used on production chips.

Demo posters were also provided by Xilinx, Cadence, Mentor Graphics, as well as the COMPLEX Project, a European project related to system synthesis methods which account for power and performance characteristics.

ESLSyn will be a yearly event, gathering the whole community related to system, HW and SW synthesis. The next conference will be organized in conjunction with DAC 2012 in San Francisco, CA. We look forward to meeting you there!

For more information on ESLsyn 2011, including the program, presentations, and proceedings as well as 2012 plans, please refer to www.ecsi.org/eslsyn

Functional Checks and Assertions Now Available to Sponsor-Level Members!

The latest comprehensive set of Functional Checks and Assertions is available now to Sponsor-Level Members. Compliance checks eliminate the need for "best-guess" verification by engineers, making certain an OCP interface complies with the specification, assuring verification quality and that IP blocks are compatible at the system level. This current set of checks supports OCP 3.0 and is now being extended for the next release of OCP, already in advanced stages of development. For your copy contact admin@ocpip.org

All Now Available!

NEW! OCP Virtual Platform (VP)

The VP is a loosely-timed model of a simple embedded platform which runs the Linux operating system. Some of the memory-mapped peripherals are modeled using the OCP Modeling Kit (OMK), further demonstrating the use of the kit. To obtain an overview and basic understanding of the Virtual Platform, please refer to our [Datashheet](#). To download a free copy of the VP, click [here](#).

Transaction Generator

The Transaction Generator (TG), is a transaction level (TL) SystemC simulator for benchmarking Network-on-Chips (NoCs) used in multiprocessor system-on-chip (SoC) applications. Utilizing this tool makes simulation of larger systems substantially faster and results obtained at this higher level can be accurately used as an initial estimate in selecting and fine-tuning NoCs. The tool is freely available through the GNU LGPL. For your copy click [here](#)

OCP Tracker

Is a software tool that provides graphical performance, statistical and transaction analysis of OCP interfaces and fabrics. It also enables validation of performance metrics via a built-in regression manager. OCP Tracker seamlessly interfaces with OCP-IP's [CoreCreator II](#) trace files to allow bandwidth, latency and other types of performance metrics to be analyzed. To request your copy of Tracker click [here](#).

IEEE 1685 Vendor Extensions

Vendor Extensions provide a way to fully describe configurable interfaces, (such as OCP) in machine-readable XML structure in an IEEE standard format. They are compatible with both IP XACT 1.4 and [IEEE1685](#). The package is available to both OCP-IP members and non-members alike. Members may access the OCP Metadata Vendor Extension package by completing the online click-through [Commercial Metadata Vendor Extension License](#). Non-Members may access the package via online click-through [research license](#).

OCP 3.0 Specification

The Specification Working Group formally released the OCP 3.0 Specification in November, 2009. This latest version contains extensions to support cache coherence and more aggressive power management, as well as an additional high-speed consensus profile and other new elements. For a copy complete our [Research License Agreement](#).

OCP Checker Now Part of CoreCreator II

The OCP checker is a fourth-generation solution for validating protocol compliance of master and slave devices using OCP. It is based on SystemVerilog Assertions (SVA) and can be used with all major logic simulators. It supports the complete set of protocol compliance checks defined in the OCP specification and spans the full range of OCP socket configuration options. The OCP checker can also generate trace files in the standard ".ocp" format for post-processing. It can be obtained, as part of CoreCreator II [here](#). For a free copy members can contact admin@ocpip.org

Debug Specification Version 1.0

The specification provides guidelines and recommended signal interfaces for on-chip debug of OCP-based systems and related multicore architectures. It describes a debug socket as a framework for IP and tools providers to develop comprehensive and re-usable debug and instrumentation environments that provide on-chip analysis and control features. These include trace, triggering, multicore synchronization, etc., along with recommendations for integration within ESL environments. For a copy of the spec click [here](#).

NoC Benchmarking Specification, Part 2 of 2

The specification presents a generic NoC architecture, a comprehensive set of synthetic workloads as micro-benchmarks, workload scenarios and evaluation criteria. These micro-benchmarks enable you to measure and pinpoint particular properties of NoC architectures, complementing application benchmarks. Click [here](#) for a copy of the spec.

NoC Benchmarking Specification, Part 1 of 2

The specification presents a modeling methodology for applications running on multicore systems and it defines an XML format for documenting and distributing NoC benchmarks. It defines a black-box view of the processing elements that discloses only the relevant computational aspects for interacting with the on-chip data transport mechanism. Click [here](#) for a copy of the spec.

OCP SystemC TLM Kits

The new kit is the first, and most advanced TLM2-based, industry-ready kit in existence today. The kits significantly increase performance, ease-of-use and ensure alignment with the OSCI 2.0.1 standard. Kits are free as part of OCP-IP membership. Non-Members may obtain a free research version. For more information contact admin@ocpip.org

Transaction Analysis Tool

The OCP Conductor Tool is an innovative, detailed OCP transaction viewer that enables fine-grained analysis of bus transactions. A complete transaction sequence can be traced from request to response, along with a host of related information about the transaction. For a free copy contact admin@ocpip.org