

OCP-IP News

Membership Announcements

Digitite - a fabless semiconductor company focused on providing high performance devices for imaging and machine vision applications.

Digitite specializes in image signal processing with multi-core processor and high level synthesis(HLS).

ProDesign - supplier of high-speed ASIC and SoC verification platforms

University of Utah – Established in 1850 this is a public research facility in Salt Lake City Utah offering more than 100 undergraduate majors and more than 90 graduate degree programs.

Xtrillion - a spin off of the medical equipment development functions and the industrial CT development functions of the US corporation TeraRecon, Inc.

From Our Partners

About D&R

Founded in 1997, D&R became the worldwide leader as a web and a B2B portal in the IP/SoC field. With its 70,000 Absolute Unique Visitors / Month (source: Google Analytics), 15,000 daily updated IP/SOC products descriptions, its news broadcast to 35,000 subscribers and the on going client/provider matching activity, D&R web stays unique worldwide.

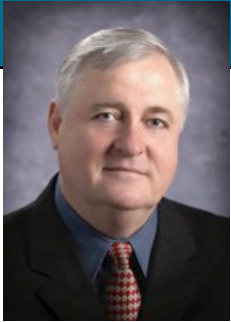
Based on its 12 years experience, D&R licenses a Java/XML multi-application, configurable enterprise platform offering the most innovative and straightforward solution for your hottest needs, including Web Product cataloging, intranet IP and Design Reuse Platform, External suppliers management, Configurable documentation ,Web support.

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SSIPEX

Shanghai Silicon Intellectual Property Exchange (SSIPEX) was founded in 2003 and is sponsored by the China Information Ministry, Shanghai Information Committee and Shanghai Science and Technology Committee. SSIPEX is a public service organization providing support to integrated circuit (IC) companies. The SSIPEX goal is to serve enterprises and government while expanding their own core business. Our mission is to promote SIP protection, SIP reuse and SIP trade. SSIPEX currently has approximately 50 employees, including experienced senior technical engineers and legal personnel with patent agent and lawyer qualifications.

President's Overview



Ian Mackintosh
OCP-IP President and Chairman

One of the advantages of working in an industry-neutral organization like OCP-IP, is the willingness of members and colleagues to share and provide information about their activities. A recent informal survey of several sellers, buyers and users of Semiconductor IP cores produced an interesting view of current business conditions and how current IP practices have morphed to meet the practical needs of addressing quality, time to market (TTM), pricing and business expediency. This President's Letter provides a brief summary of those discussions.

At the outset we should reflect on a great peculiarity of the IP market: it is a striking fact that opinions shared and actions taken in the use and purchase/sale of IP are massively colored by, "the function and functionality of the IP, who is the buyer (or, seller) and what is the IP's end use." Having said that, the following commentary relates only repeated themes, comments and observations and finally reflects upon the likely industry changes these issues will effect over the next 5-10 years.

Firstly, let me comment on general SoC design activity, uniformly related to myself by numerous suppliers as I repeated my own enquiries over the last several months. In late 2QCY09, new design activity was generally considered "frozen," but by the early days of 3QCY09 the common report was of there being new business, but "it is very hard to close and often repeat/contract renewal activity at legacy accounts." By middle-late 3QCY09 design-starts were reportedly more generally occurring, but these were almost exclusively derivative designs and by 4QCY09 there were finally some comments that developers of these designs were now communicating the belief that there would be more (derivative) designs to follow. Finally, by end 4Q there were early reports of design-starts on original designs. Given many IP providers service consumer segments (and this would impact the forgoing commentary), we will see these increasingly active

customers either progress more generally to original design-works, continue focus upon derivative work, or, "close down again" as the seasonal-cycle passes and/or we enter the realities of the new (2010) budgeting/planning cycle. Overall, it is reported that a very slow recovery is already underway, although IP providers still complain of excruciating pain extracting money from users (despite there being comparatively less difficulties doing so in Military, Medical and AMS Market segments).

On the topic of IP-core quality, both users and providers are uniformly open and in agreement. There are quality issues in the IP being supplied. At the low-end of IP for FPGA's there are horror stories of missing test benches and basic documentation, yet even in "high end" cores (not including those few, rare "Star IP" cores in this commentary) problems are occurring. These are often driven by usage issues, where even very mature (and hardened) IP exhibits flaws when deployed in new and stressful applications. Configurable IP too, can be particularly prone to bugs as exhaustive verification of such functions is often impracticable and/or too costly to justify. Users are aware that suppliers often have IP-dependant quality issues and correspondingly, one good IP does not guarantee uniform quality from a supplier, even if that quality IP core is of star quality. It seems that the old adage, "IP quality will be determined by use" is often a good measure. So, with this backdrop, the user-community has adopted a relatively common process to secure their own objectives.

When IP cores are acquired by SoC developers they undergo an evaluation phase ahead of any purchase, which largely decouples the function's quality issues from the critical development path. In most Tier 1, 2 and some tier 3 accounts after initial budgetary scouting, an engineering group will exercise an IP for typically 2-4 weeks

Presidents Overview (Continued)

by verifying, testing, exploring its behavior and functionality in their (sub) system and environment, etc. The contractual process will then pick-up again later, just before the main project engages and the core needs to be deployed. Interestingly, most Tier 1 suppliers have extensive internal IP standards (for packaging, delivery, testing, verification etc. etc.). However, it is almost always the reported case that no attempt is made by such companies to impose such standards upon suppliers, rather the focus is upon “what do you have and what will it take to integrate.” This lack of pressure from users may even be fortuitous, as there is no real uniformity between the internal IP standards held between these companies and although this undoubtedly eases the burden on suppliers, it unfortunately just as certainly affects quality. Generally, the central R&D groups pushing internal standards in such user-companies seem to be viewed as out-of-touch with the real integration needs and operation of SoC development teams. Overall, the industry adoption of this off-line evaluation process can (to a degree) “protect” SoC developers, certainly from gross quality issues, but will not always avoid issues related to exhaustive application requirements, nor protect those user-communities unable make any serious level of proactive evaluation. What is most alarming are the gross repetition, risk and duplication of effort wasted in this process adaptation, and all for the lack of industry cooperation on shared standards.

Over on the contractual front there are other interesting issues. Despite common beliefs, the rationalization of Royalties versus License fees is not a *general* impediment in IP sales. Providers either have IP that commands Royalties, or they do not, so this conflict should always self-rationalize in the purchasing process. Also, the evaluation/purchasing process we see above, is normally run outside the critical path of SoC development. Despite this, the most serious and common problem reported today in contractual delays is the legal resolution of nuances relating to IP rights, indemnification etc., and this particularly so where Asian and Western buyer-sellers are engaged. Where contractual problems do stretch out for months (and no alternative suppliers are engaged) and developments are predominantly centered around derivative designs with inherently shorter TTM requirements (typ. 2-3 month for SoC's), then such issues become either major headaches or business leverage opportunities, depending upon whether you're buying or selling the IP. The reported purchasing cycles for technical evaluation phases by buyers of IP run typically 2-6 weeks with the overall purchase commonly completing after 3 months. Purchases in the Military segment typically take 3-6 months from start to finish. Finally, it should be noted that a common supplier complaint is that customers will

not pay for quality and low-quality (and often lowest-bid) suppliers continue to set the pricing expectations in many sales transactions.

It remains to consider the future for the IP Market and what might change over the next 5-10 years. The problems and issues noted above, along with general industry maturation suggest we should expect changes on many fronts. Namely, it's difficult not to envision a progression of CONSOLIDATION in the SoC IP supplier base as the big get bigger, both investment money supply and the IP Market remain soft and the potential for IPO's is small. In addition, integration is the cornerstone of electronics and so we should also expect LARGER IP's or IP SUB-SYSTEMS being offered increasingly, as suppliers strive to add value and expand their opportunities in the video, sound and general multi-media space. Expect to see large groupings of currently stand-alone IP Cores offered with software, drivers and debugging schemes, etc. It is also likely FOUNDARIES will take on an expanding position and leverage their closeness to silicon hardening with pricing and capacity advantages, much as Synopsys bundles IP products with Design Compiler, today. QUALITY should continue to improve, even if driven by nothing other than legacy core usage, with maturing vendor-user relationships and coordination; vendors will either provide improving product quality or fall off supplier lists. Next, LICENSING CYCLES can decrease as the effects of both vendor consolidation and shortened, “preferred-vendor” lists consequently improve supplier coordination, and all this will be further fueled by annual purchasing schemes and “all-you-can-eat” business arrangements. Lastly, as more users cease to be able to afford the costs of SoC's, growing FPGA usage will most likely play a prominent role in driving standards increasingly heavily into IP core deliverables, since increased ease-of-use will prove essential support for a huge and growing FPGA design community.

This snapshot of the IP Market today shows it has already significantly morphed and adapted throughout the last decade and exposes reasons why it must inevitably continue to change. It's clear that the practices, progress and issues we already observe will continue to ensure a similarly rapidly changing landscape for the IP Market in the coming 5-10 years.



OCP-IP 2.2 MVC Accelerates Verification Productivity

*Mark Peryer – Verification Practice,
Mentor Consulting*

In April 2009, Mentor Graphics released the 2009.1 version of its Multiview Verification Component (MVC) library which featured an upgrade to its OCP-IP MVC to make it OCP-IP 2.2 compliant. The OCP MVC also supports the OCP 3.0 disconnect and WR_NP without write_response enable features. Another major feature of the 2009.1 version of the MVC library was that it was re-packaged to align the MVCs with version 2.0 of the SystemVerilog based Open Verification Methodology (OVM).

The OCP MVC, like every component in the MVC library, comes with a comprehensive kit of parts and supporting files. The OCP MVC can be configured to be used as either an OCP Master or an OCP Slave. The OCP master can be used to generate OCP compliant stimulus for an OCP slave using OVM sequences to generate bus requests. The MVC OCP slave acts as a responder which means that it is able to return an OCP compliant response to a bus request; again OVM sequences can be used to model the behaviour of the responder. Both the OCP master and slave components have protocol checking built into them which checks for malformed responses to requests. However, for exhaustive checking, the Questa Verification Library (QVL) OCP-IP protocol monitor packages up a set of assertions which checks the validity of OCP transfers on the bus.

The OCP-IP MVC comes with an OVM Monitor component that emits different transactions according to which bus events occur. These transactions can be used with either a functional coverage monitor or a scoreboard to build up a picture of which OCP transfer types

have occurred or to check the behaviour of a system. A set of example environments is also supplied as part of the kit to illustrate how to use the OCP-IP MVC and implement verification environments with it. One of these example environments is an exhaustive OCP-IP bus compliance test which can be adapted to a target architecture by changing its constraints. A verification plan that is compatible with Mentor's Questa verification tracker is also supplied to make it easier for users to prove that they have checked all applicable modes of operation, or that a particular test case has exercised the expected set of transfer formats. Again, this plan can easily be adapted to suit the specifics of a particular system. Mentor's Consulting group has implemented a number of customer verification environments based on the compliance example and has found that it can be productive in finding protocol implementation bugs in a matter of hours.

The 2009.1 release of the OCP MVC has been re-packaged to align it with the SystemVerilog OVM 2.0 verification component base class library. The effect of this is that it has become straight-forward to implement an OVM verification environment that incorporates a MVC. The foundation of the OVM is an Open Source SystemVerilog class library that allows end users to quickly put together a productive verification environment based on clearly defined interfaces between verification components and a stimulus generation regime that separates test case implementation from the test bench. The methodology behind the OVM is a fusion of Mentor's AVM and Cadence's eRM/uRM which encapsulates the verification

OCP-IP 2.2 MVC Accelerates Verification Productivity (Continued)

experience of both companies.

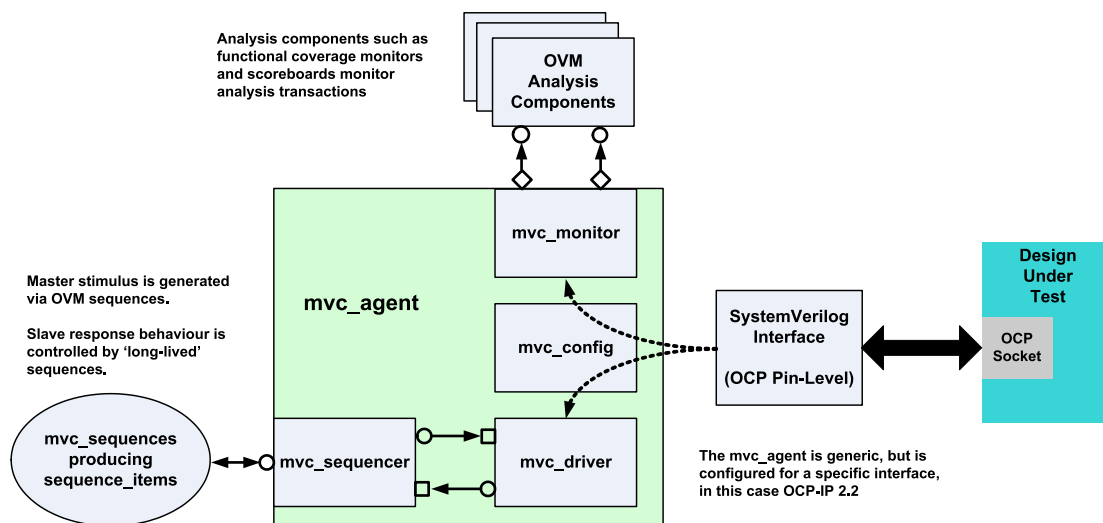
Environments implemented using this library can be run on any IEEE 1800 compliant simulator. The OVM has a substantial and growing user base, some of whom have formed a steering committee to guide the roadmap for future versions of the OVM base classes. More details about the OVM and the source code for the OVM package itself can be found at <http://www.ovmworld.org>.

The major challenge of developing verification IP (VIP) for the OCP-IP 2.2 standard is that there are an almost infinite number of possible interface behaviours that can be defined using the OCP-IP parameters. This requires that an OCP VIP be easily configured to meet all potential use cases. In addition to this behavioural aspect, the verification component must be parameterizeable in order to accommodate variations in the width of bus fields and the presence or absence of different sideband signals. This calls for a flexible approach to VIP configuration which in the case of the OCP MVC is done using a SystemVerilog

class to capture all of the possible properties that might be used to describe the behaviour and parameters of an OCP interface. For ease of use, the names of the protocol specific parameters used naturally match those defined in the OCP-IP standard.

The generic structure of a MVC is illustrated in Fig 1. All MVCs use a common `mvc_agent` class which always contains the same active component classes. The active part of an MVC is always contained within a SystemVerilog interface, which is connected to the pins of the design under test. The classes within the MVC agent are passed a configuration class object which encapsulates details of the set-ups for the MVC interface and, most importantly, a pointer to the MVC interface itself. This object is then used by the MVC agent to configure itself and its sub-components to behave in the correct way.

To read the entire article, click [here](#) ...



Generic MVC_Agent structure

SOLV: Available to OCP-IP Members

OCP-IP released SOLV (Sonic’s OCP Library for Verification) as a FREE part of paying membership entitlement in November 2008. SOLV consists of three Verification components – OCP Protocol Checker, OCPdis2 and OCPperf2. The tool flow for the SOLV package is shown in Figure 1.

Open Core Protocol

The Open Core Protocol (OCP) is a public standard memory-mapped core interface. It is defined by collaboration between system houses, electronic-design-automation (EDA) vendors, and intellectual-property (IP) suppliers within the OCP International Partnership (www.ocpip.org). The motivations for defining the OCP are to enable better IP reuse and a wide spectrum of common tooling and experience.

OCP is a rich standardized interface and can support a wide range of cores. The interface is highly configurable and can adapt to the needs of various cores. The diverse nature of the interface can easily allow for the various combinations of cores used within the industry today.

The OCP Functional Verification Working Group (FVWG) has developed a set of protocol rules for protocol compliance which have been documented in Chapter 18 of the OCP 3.0 specification. OCP Protocol Checker has been implemented to cover all these rules as described in this chapter of the OCP specification. The OCP Protocol Checker has been regressed across all Sonics IP’s that support an OCP interface and has been used internally by Sonics for over 5 years. It has also been shipped to all

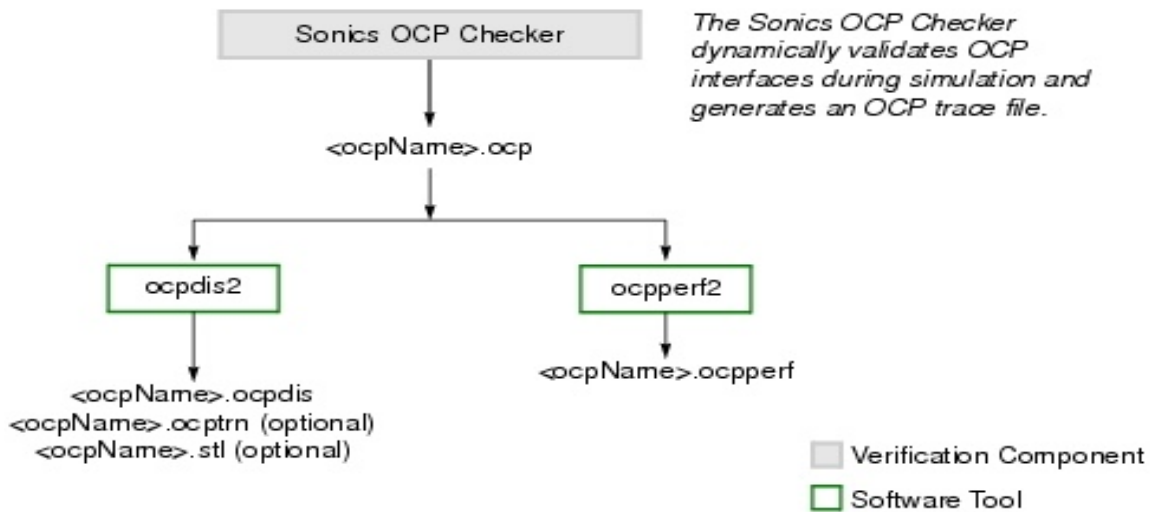


Figure 1 SOLV tool flow

Continued next page

Sonics customers with the verification testbench provided as part of Sonics IP deliverables. Hence the protocol checker has attained a great level of maturity over the last 5 years and has become an integral verification component for Sonics and many of our customers.

Assertion Based Verification and SVA

Assertion Based Verification (ABV) Methodology has been adopted and used by the verification community extensively in the last decade. For SoC interfaces, ABV is a natural choice. With a defined protocol rule set, ABV can facilitate bug identification due to illegal behavior in the interface. System Verilog Assertion (SVA) language is a very robust language for ABV. SVA is widely accepted in the industry and the tool support for debugging assertions is very robust and mature. The OCP Protocol Checker was developed using ABV Methodology and SVA language.

OCP Protocol Checker

A significant amount of debug time is spent on the interfaces that are developed in-house for System-On-Chip (SoC) designs. With increasing complexity of original and derivative SoC designs it is imperative to use both a standard interface and also debug capabilities supporting the interface. OCP Protocol checker from Sonics can be easily plugged into multiple OCP interfaces used in the SoC testbench. The SOLV manual lists the steps required to connect the OCP protocol checker to the OCP interfaces in any given SoC design.

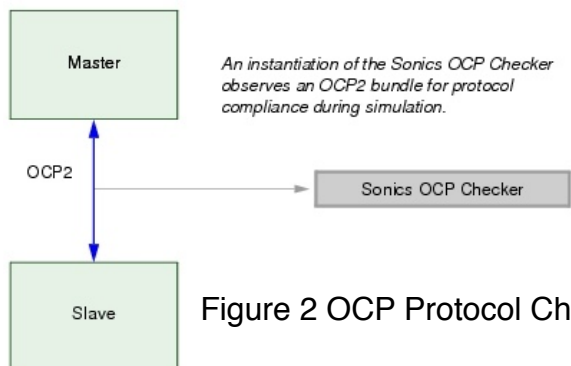


Figure 2 OCP Protocol Checker

Following is an example instantiation of the Sonics OCP checker to the interface. Each checker instance will have instance parameters and protocol parameters. Example instance parameters are: (a) number of cycles for the interface to be idle and (b) maximum number of outstanding requests in the interface. The SOLV documentation can be referred to for additional parameters that can be controlled by the user.

```

ocp2_sva_checker #(
    //Instance Parameters
    .version ("

```

The “Protocol Parameters” section needs to match the OCP configuration information of the interface. Parameters that are not used in the interface need to have default values. The next step is to instantiate the checker port for each interface in the testbench.

```

checker_port (
    .Clk_i (Clk),
    .Mcmd_i (Mcmd),
    .MAddr_i (MAddr),
    ...
    ...
    .MBurstSeq_i (1'b0),
    .MBurstSingleReq_i (1'b0),
    ...
    ...OCP Protocol checker instantiation

```

It is important to note that signals that are not used in the interface need to be tied off low. An example is MBurstSeq_i and MBurstSingleReq_i in the code above. The checker is supported with Incisive NCVERILOG, VCS and Modelsim simulators. The user needs to perform the above steps and OCP Protocol checker reports any mismatches in the protocol during the simulation

run. An example protocol error mismatch is shown here:

```
# ** Error: PROTOCOL: D096: SRespLast was
asserted for a non-last response phase
# Time: 274434 ns Started: 274434 ns Scope:
stim.McBpR_256DS.ocpmon.ocpmon_ocpmon2_s
va.threaded_checks[0].genblk11.ap_D096
```

The error message prints out a message explaining the error, time of the error during the simulation run and the hierarchical path of the OCP instantiation for which the error was reported. The information provided in the error message is very useful for the engineer debugging the SoC enabling him to isolate the interface and hence provide a starting point for debug.

Ocpdis2 and OcpPerf2

Along with the OCP protocol checker, the SOLV package also provides two programs that help with debug and performance: Ocpdis2 and OcpPerf2 (Figure 1). OCP Protocol Checker is capable of generating traces for each interface and the user has the capability to enable the generation of traces during setup time. The Ocpdis2 program could be run on the traces and the generated output can then be used to debug the transactions. An example disassembled file is shown in here

```
##
## Generated by ocpdis2 1.7
##
# Legend for 'transfer' output style (sorted by
request cycle)
# -----
##
# SimTime : Simulation Time | Time
# Cycle : Cycle Valid Time | Cycle
# Cmd : Master Command | MCmd
# BuS : Master Burst Sequence | MBurstSeq
# Burst : the running transfer count / Master Burst
Length x Master Block Height / Master Block
Stride | transfer count/ MBurstLength x
MBlockHeight/MBlockStride
# L : Master Last Request | MReqLast
# RL : Master Row Last Request | MReqRowLast
# AS : Master Address Space | MAddrSpace
# Addr : Master Address | MAddr
# Data : Data | Data
# Resp : Slave Response | SResp
# SL : Slave Last Response | SRespLast
# SRL : Slave Row Last Response |
SRespRowLast
```

```
SimTime Cycle Cmd BuS Burst L RL AS Addr
Data Resp SL SRL
-----
790 79 WR BLCK 1/2x3/8 0 0 1 29929dcd4fbfe8
ad4fbfe8
800 80 WR BLCK 2/2x3/8 0 1 1 29929dcd4fbfec
ad4fbfec
810 81 WR BLCK 3/2x3/8 0 0 1 29929dcd4fbff0
ad4fbff0
820 82 WR BLCK 4/2x3/8 0 1 1 29929dcd4fbff4
ad4fbff4
830 83 WR BLCK 5/2x3/8 0 0 1 29929dcd4fbff8
ad4fbff8
840 84 WR BLCK 6/2x3/8 1 1 1 29929dcd4fbffc
ad4fbffc
850 85 RD BLCK 1/1x3/8 0 1 1 29929dcd4fbfe8
ad4fbfe8 DVA 0 1
860 86 RD BLCK 2/1x3/8 0 1 1 29929dcd4fbff0
ad4fbff0 DVA 0 1
860 86 RD BLCK 2/1x3/8 1 1 1 29929dcd4fbff8
ad4fbff8 DVA 1 1
```

The disassembled output is useful for an engineer debugging the SoC as it allows him to identify the traffic pattern that resulted in the mismatch. The disassembler can produce the generated file in wire style, transfer style, transfer-data style and STL style. OcpPerf2 is used to measure Bandwidth, Latency, etc. SOLV documentation can be referred to for the available options which allow for measuring the performance on an OCP interface. A textual file (similar to Figure 6) would be generated with the performance results for an OCP interface.

This article explained the steps involved in utilizing the SOLV software package to: instantiate the OCP Protocol Checker, debug OCP Interfaces, visualize traffic patterns and generate performance numbers. OCP Protocol Checker uses Assertion-based verification methodology and also is supported by the three leading industry simulators. The package is extremely useful for SoC debug and compliments existing debug techniques already available to the industry.

Working Group Updates

Meta Data Working Group:

The Metadata Working Group (MDWG), continues to finalize the enhancements to fully capture OCP interfaces using the IP-XACT format defined by SPIRIT Consortium. The extensions describing OCP within existing IP-XACT format have gone to the Governing Steering Committee for approval and will be available to OCP-IP members by 1QCY10. The MDWG is also creating OCP configuration and interface compatibility checkers.

Debug Working Group:

The Debug WG focus heading in to 2010 is in identifying required instrumentation signaling extensions and example cases for debug of multi-core systems that support OCP 3.0 cache and power management features. These may include SMP, AMP, multi-threaded, and other system architectures. Preliminary goals are for OCP 3.0 compatible debug systems white papers to be published in 1QCY10 with updated specifications to be developed later in the year.

Specification Working Group:

The Specification group recently released OCP 3.0 which now includes the additions of cache coherence extensions, power management signaling, a write response extension and a third consensus profile. OCP 3.0 became the official specification of record in 4QCY09. Be sure to watch future editions of the OCP-IP newsletter for announcements about future plans for the Spec Working Group.

NoC Benchmarking Working Group:

This working group is currently profiling the EEMBC MultiBench programs on an FPGA-based multiprocessor system. The system is composed of multiple soft core processors, network-on-chip with built-in monitoring capabilities, DDR controllers, and shared SRAM. Some effort is needed to port the benchmark programs that were originally targeted for server environment. Progress on this work is proceeding in a timely fashion.

System Level Design Working Group:

The SLD's project to evolve and enhance the entire Transaction Level Modeling kit and support modeling is now complete, OSCI 2.0 compatible, and is available FREE from our website. The next release of this kit focuses on alignment with the OSCI TLM-2.0.1 release, keeping compatibility between the OCP SLD kit and the OSCI TLM standard. The group is now focused on further advancing the TLM Kits to include support for the new features defined in OCP 3.0. The next phase of the kit advancement includes collaboration with a strategic partner focused on software needs for semiconductors.

Functional Verification Working Group:

Following the official availability of OCP 3.0 release in 4QCY09 the group has begun formal meetings and work in support of the latest revision of the specification.

Marketing Working Group:

The Marketing Working Group has recently completed presentations at the TSCUG Conference in Taiwan and at IP/ESC '09, Grenoble France. In addition, we remain very active helping member companies compose and place their OCP-related articles and conference papers, while publishing the OCP-IP newsletter and our regular press releases. If your company would like assistance placing an article, prominently targeted to the industry or directly to our OCP-IP focused community, please contact admin@ocpip.org.

Development OCP wrapper for non-OCP reuse IP cores

By: NGUYEN The Dai Duong, DANG Trong-Trinh, ICDREC, VIETNAM

Two requirements for the design community are shortening the development schedule of SoC by reusing IP cores and adopting a standard and well-defined interface protocol to ease the interconnection of third-party IP cores during the design process. The Open Core Protocol (OCP) satisfies these two requirements. OCP enables both true plug-and-play and re-use. Furthermore, this is OPEN standard.

The OCP approach (similarly used by the Virtual Socket Interface Alliance's (VSIA) Design Working Group on On-Chip Buses) is to specify a bus wrapper to provide a bus-independent Transaction Protocol-level interface to IP cores. The OCP is a modern, functional superset of VSIA's Virtual Component Interface (VCI). While the legacy and now retired VCI approach addressed only data flow aspects of core communications, the OCP additionally supports configurable control signaling and test signals. The OCP is the only standard that defines protocols to unify all of the inter-core communication.

The OCP defines a bus-independent interface between IP cores that reduces design time, design risk and manufacturing costs for SoC designs. An IP core can be a simple peripheral core, a high-performance microprocessor, or an on-chip communication subsystem (a wrapped on-chip bus). With these aspects, the open core protocol:

- achieves the goal of IP design reuse. The OCP-compliant IP core is independent of the architecture

and the design of the systems in which they are used.

- optimizes die area by configuring OPC-compliant IP cores into the OCP system only those features needed by the communicating cores.
- Simplifies system verification and testing by providing a firm boundary around each IP core that can be observed, controlled, and validated.
- eliminates the task of repeatedly defining, verifying, documenting and supporting proprietary interface protocols.
- adapts to support new core capabilities while limiting test suite modifications for core upgrades.

The OCP protocol flexibility, configurability and scalability are the key elements making OCP massively used and successful in major electronics markets. Because of these characteristics any IP can utilize the best signals for the connection to the OCP backbone with immediate benefit for bandwidth capability. This has made OCP broadly used in many applications like multimedia, telecom, gaming, and other areas.

Reusable IP cores can be designed and implemented to be compatible with OCP directly by using the OCP specification. For existing IPs, supporting other interface standard (such as AXI protocol, Avalon, etc), an OCP wrapper must be developed. This article shows how to develop the OCP wrapper for a reusable microcontroller IP - SigmaK3.

To read the complete article visit [here](#)

Recent Publications

Available in the [OCP-IP Press Room](#)

Press Releases

November 19 - [OCPIP releases 3.0 specification](#)

Articles

November 09 - [The best of both worlds: Optimizing OCP slave memory behavior EE Times/DesignLine](#)

**October 27 [IP Industry Review](#) by Ian Mackintosh
EE Times**

**October 06 - [OCP 2.2 MVC accelerates verification productivity](#)
EE Times-EDA Design Line**

October 02 [STEP - Automated Synthesis of On-Chip-Bus Protocol Transducer](#)

Announcements: Now Available

NEW! OCP 3.0 Specification

The Specification Working Group officially released the OCP 3.0 Specification in November. This latest version contains extensions to support cache coherence and more aggressive power management, as well as an additional high-speed consensus profile and other new elements.. For a copy complete our [Research License Agreement](#).

OCP Checker Now Part of CoreCreator II

The OCP checker a fourth-generation solution for validating protocol compliance of master and slave devices using OCP. It is based on SystemVerilog assertions (SVA) and can be used with all major logic simulators. It supports the complete set of protocol compliance checks defined in the OCP specification and spans the full range of OCP socket configuration options. The OCP checker can also generate trace files in the standard “.ocp” format for post-processing. The checker can be obtained, as part of CoreCreator II [here](#).

Debug Specification Version 1.0

The Debug Specification provides guidelines and recommended signal interfaces for on-chip debug of OCP-based systems and related multicore architectures. It provides a framework for IP and tools providers to develop comprehensive and re-usable debug and instrumentation environments that provide on-chip analysis and control features. These include trace, triggering, multicore synchronization, etc., along with recommendations for integration within ESL environments. For a copy of the spec click [here](#).

Network-on-Chip Benchmarking Specification, Part 2

Part 2 of the two-part NoC Benchmarking Specification presents a generic NoC architecture, a comprehensive set of synthetic workloads as micro-benchmarks, workload scenarios and evaluation criteria. These micro-benchmarks enable you to measure and pinpoint particular properties of NoC architectures, complementing application benchmarks. For more information, [click here](#).

Network-on-Chip Benchmarking Specification, Part 1

The specification presents a modeling methodology for applications running on multicore systems and it defines an XML format for documenting and distributing NoC benchmarks. It defines a black-box view of the processing elements that discloses only the relevant computational aspects for interacting with the on-chip data transport mechanism. Download our [NoC white paper](#) for more information

Transaction Analysis Tool

The Tool is an innovative, detailed OCP transaction viewer that enables fine-grained analysis of bus transactions. A complete transaction sequence can be traced from request to response along with a host of related information about the transaction. For a FREE copy contact admin@ocpip.org

OCP SystemC TLM Kits

The new kit is the first, and most advanced TLM-2.0 based, industry-ready kit in existence today. The kits significantly increase performance, ease of use and ensures alignment with the OSCI 2.0 standard. The kits are free as part of OCP-IP membership. For more information contact admin@ocpip.org