

OCP Verification IP Overview

Neill Mullinger
VIP Product Manager

Synopsys Verification IP Portfolio

- **Common infrastructure / usage style**
 - Simplifies multiple-model usage
 - Easy to learn new titles
- **Supports wide variety of EDA environments**
 - Integrated in Synopsys Discovery™ platform
 - Native for higher performance
 - Verification Methodology Manual (VMM) support
 - Accellera SV-UVM compatible
 - Supports all popular simulators
 - Verilog task-based interface

Current Protocols

AMBA 3 (AXI, APB3)

AMBA 2.0 (AHP, APB)

OCP (3.0, 2.2, 2.1, 2.0)

PCI Express (3.0, 2.1, 1.1)

USB 3.0 (SS, HS, FS, LS)

USB (2.0, 1.1, OTG)

PCI/PCI-X (2.3, 2.0)

SATA (1.5, 3.0 and 6Gbps)

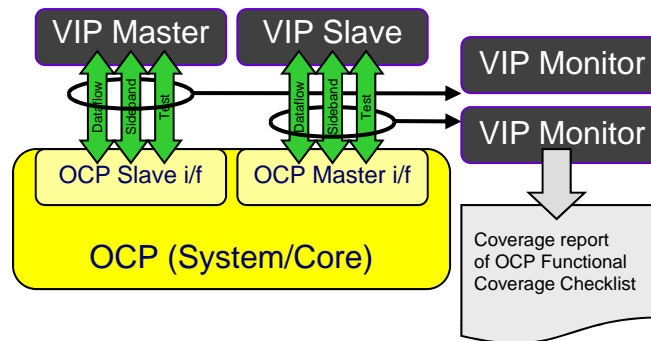
10/100/1G/10G Ethernet (GMII, XAUI, SGMII, RGMII, etc.)

Serial I/O (RS232, GPIO, IrDA)

I2C

DW OCP Verification IP

*Supports all OCP 2.0/2.1/2.2 dataflow & sideband transaction types
New 3.0 features support*



- Master initiates OCP transactions
- Slave observes the master-driven signals on the bus and initiates response procedure
- Monitor observes and reports on OCP bus activity
 - Built-In Functional Coverage of OCP-IP defined functional coverage groups
- Configuration determines which signals are in interface, how wide they are, number of concurrent transfers, timeouts, burst length, burst type etc

OCP 3.0 Support

- Configurable for USB 3.0 or 2.2
 - Default is 2.2 behavior
 - User parameter sets to 3.0
- OCP 3.0 support
 - Power Management
 - Connection/Disconnection Protocol Support
 - Reordered Responses for Transactions with Overlapping Addresses
 - Supports both types of ordering responses
 - WRNP and WRC Transactions Legal when writresp_enable is 0

Verification Plan

Full OCP-IP Spec Coverage

feature	subfeature	subfeature	subfeature	subfeature	subfeature	subfeature	subfeature	value dw_ocp.group
Functional Coverage								45.12%
	OCP Spec 2.2-1.1							45.12%
		Section 16						45.12%
			Mandatory					62.73%
				Dataflow				62.73%

- Test Plan
 - Derived from specification and protocol-specific coverage groups
- Automated back-annotation of coverage results

subfeature+	subfeature	sub-feature	value dw_ocp.group
Transaction Coverage			71.62%
	trans_cross_trans_TypesResults		85.93%
		TransTypes	93.33%
		SResp	100.00%
		cc	64.44%
	trans_cross_trans_TypesBurstPropsBytes		73.17%
		TransTypes	93.33%
		MAtomicLength	57.81%

Results

Coverage Bins

How we test DesignWare OCP VIP

Internal Regression Environment

- Constrained Random Verification
 - Randomized traffic
 - Randomized configurations
 - Some directed tests
- Covers 100% of mandatory coverage points
 - As described in the OCP functional spec
- Regression Environment is used as a basis for the testbench example shipped with the Verification IP
 - Includes scenario generators to aid testbench development
 - Includes examples of the tests



DW Verification IP for OCP endorsed by OCP-IP

- DW VIP for OCP included with CoreCreator and available to paid-up members of OCP-IP.
 - Each paying member company of OCP-IP in good standing is entitled to three no-charge licenses of DesignWare Verification IP for OCP as part of their subscription benefits
 - DW OCP Monitor generates OCP trace file format for use with CoreCreator post processing tools
- Member companies may request the licenses from the OCP-IP website and download the VIP from the Synopsys IP director

Announcement

Not for Release Until April XX, 2007

OCP-IP STANDARDIZES ON SYNOPSIS' DESIGNWARE VERIFICATION IP FOR OCP-IP'S CORECREATOR VERIFICATION TOOLSET

*Collaboration Delivers OCP-compliant Verification
Solution for Improved Interoperability and Quality of OCP designs*

MOUNTAIN VIEW, Calif. and BEAVERTON, OR – April XX, 2007 - Synopsys, Inc. ([Nasdaq:SNPS](#)), a world leader in semiconductor design software, and Open Core Protocol International Partnership (OCP-IP), an independent non-profit semiconductor industry consortium, today announced that they are collaborating to provide Synopsys' DesignWare® Verification IP (VIP) as part of OCP-IP's CoreCreator verification toolset. DesignWare VIP for OCP, part of Synopsys' portfolio of standards-based verification IP, will become the OCP-IP endorsed verification IP solution and will replace the OCP Bus Functional Models (BFM) currently provided with [OCP's](#) CoreCreator tool. The new, combined solution, which includes DesignWare VIP and [CoreCreator's](#) performance analysis, protocol checking, and transaction disassembly, gives OCP-IP members a common verification toolset, enabling maximum consistency and interoperability across OCP implementations. The collaboration also further expands OCP-IP's robust thriving infrastructure.

Synopsys Verification IP Benefits

- **Saves testbench development time**
 - Easy to integrate into your current methodology
 - Includes coverage reports and protocol checks
- **Reduces project risk**
 - Verifies full breadth of each protocol
 - Supports SystemVerilog constrained random verification
- **High quality**
 - Design proven on hundreds of customer designs
 - Extensive regression environments
- **Broad Verification IP Portfolio**
 - Most popular protocols for SoC Verification

