

# Introducing the MIPS32® 1074K™ Superscalar Coherent Processing System (CPS)

*Selected Slides, March 2011*

For more information, contact  
[info@mips.com](mailto:info@mips.com)

# MIPS32® 1074K™ CPS Highlights

*Fastest fully synthesizable licensable multicore IP  
→1.5GHz 40nm (w.c.); scales to 2.5GHz 28nm (typ.)*

*Compelling JavaScript and Web performance  
for digital home applications*

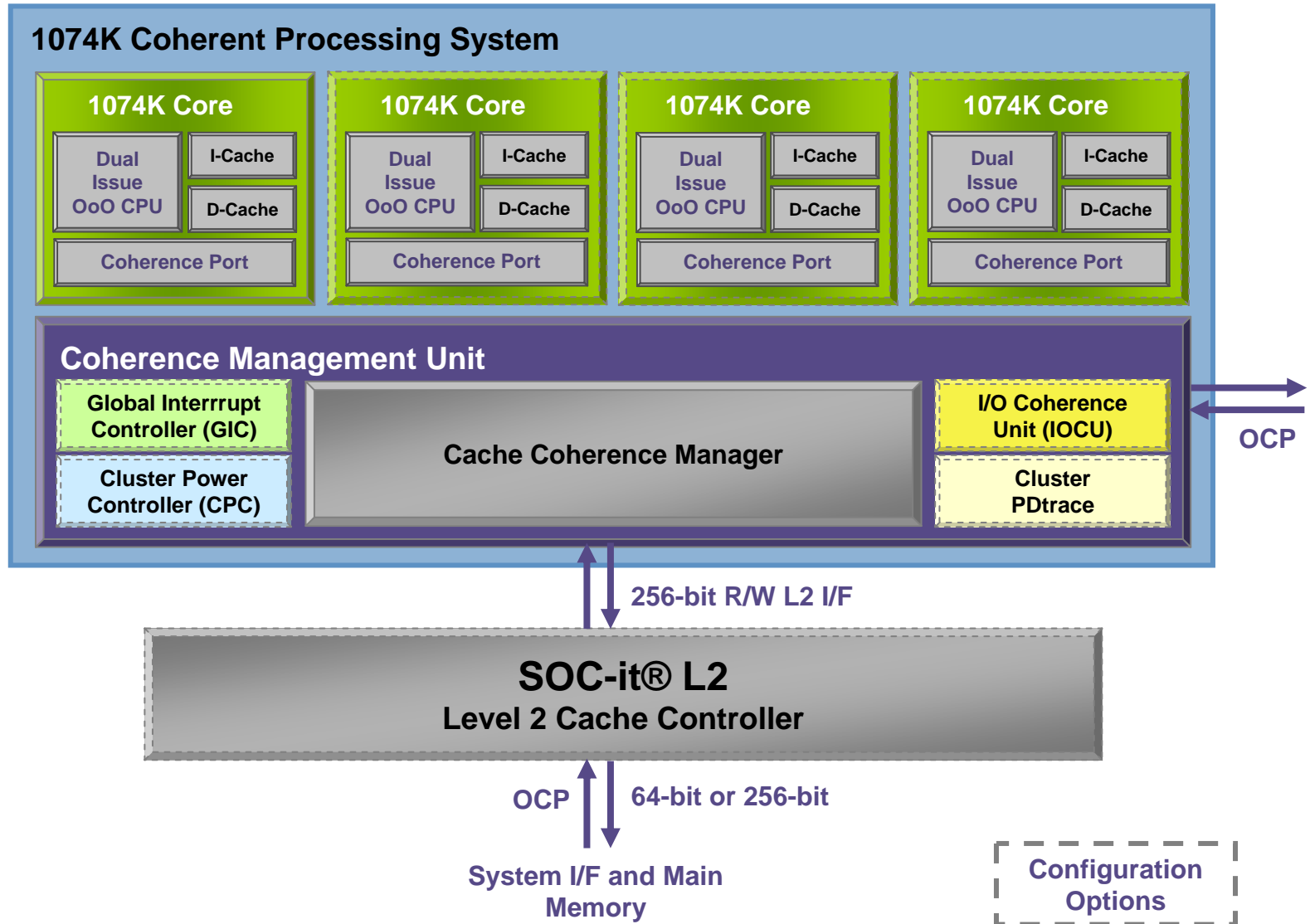
*Extends MIPS' heritage in multiprocessing platforms*

*Strongly leveraged ecosystem: binary-compatible  
with MIPS32 24K® and 74K® series*

*>15,000 CoreMark and >12,000 DMIPS in  
4-core implementation in 40nm*

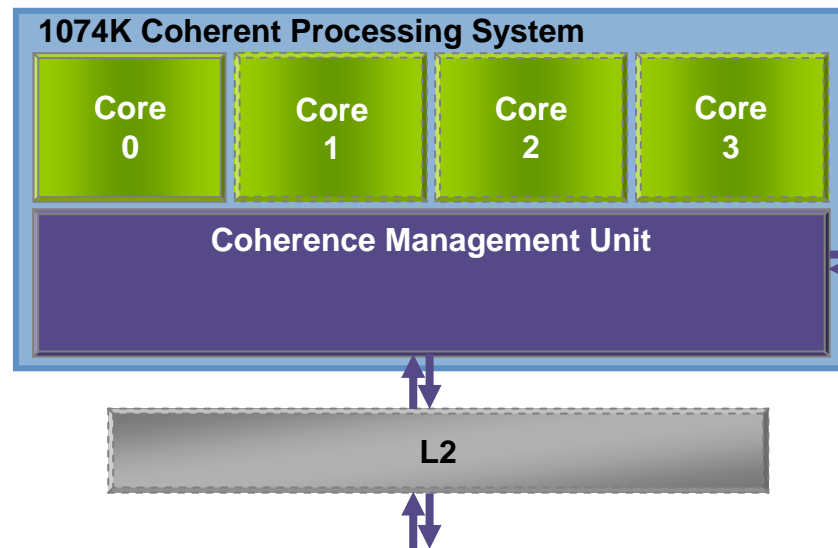
# 1074K Coherent Processing System (CPS)

At the core of the user experience.®



# 1074K CPS Optimized for Data Movement

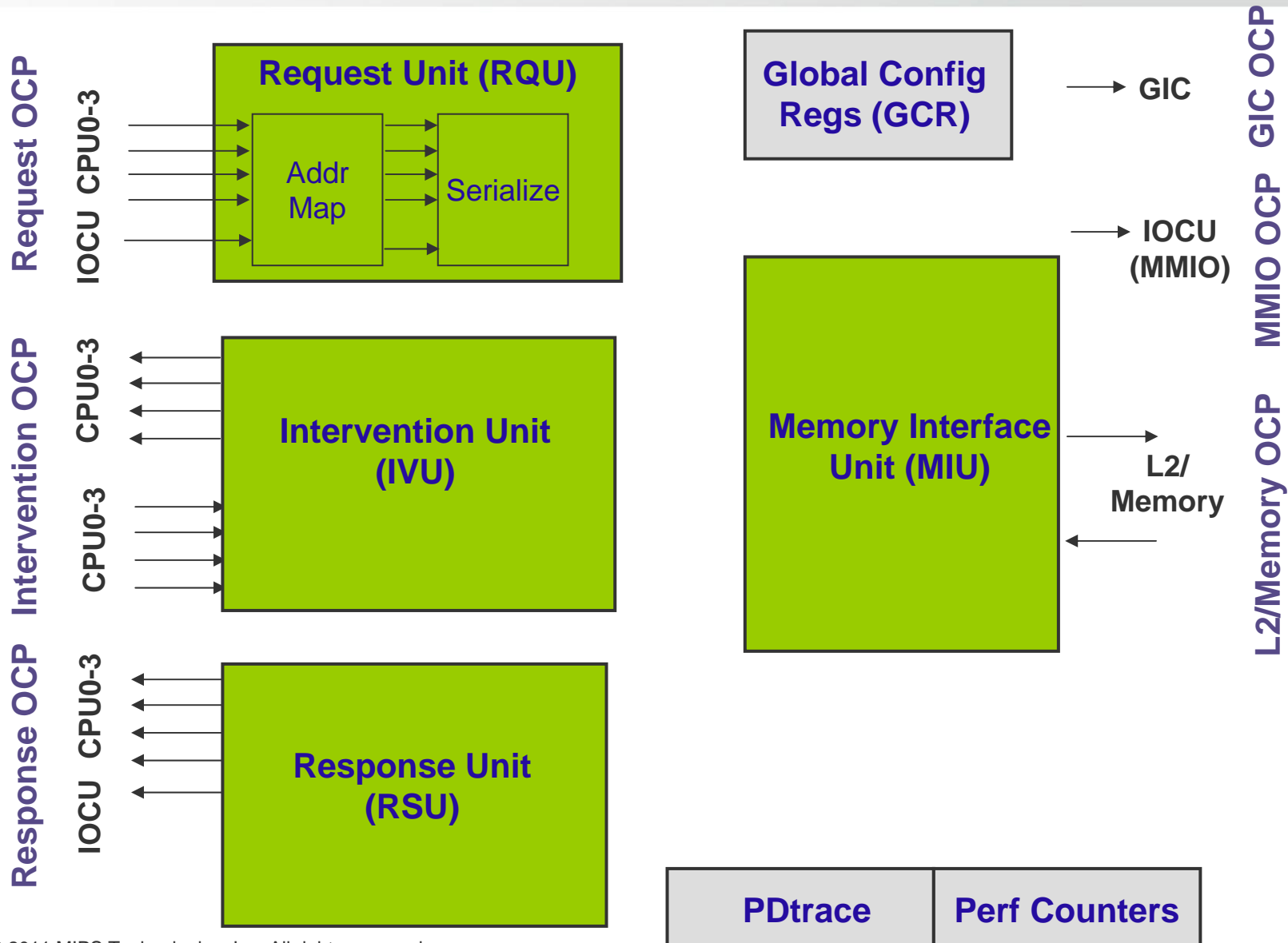
- ❖ **High bandwidth fabric**
  - Key datapaths are 256b wide
  - Optimized interface transfers full 32B line on L2 hits
- ❖ **Speculative memory reads**
  - Start L2/mem read before intervention responses
  - Reduces effective memory latency
- ❖ **Cache to cache transfers**
  - Exclusive or modified data transferred directly from another L1 cache
  - Some upgrades can be data-less
- ❖ **Hardware IO Coherence**
  - Efficient handling of IO data shared with core caches
  - Controllable L2 allocation



# 1074K Coherence Manager (CM)

## High-Level Architecture

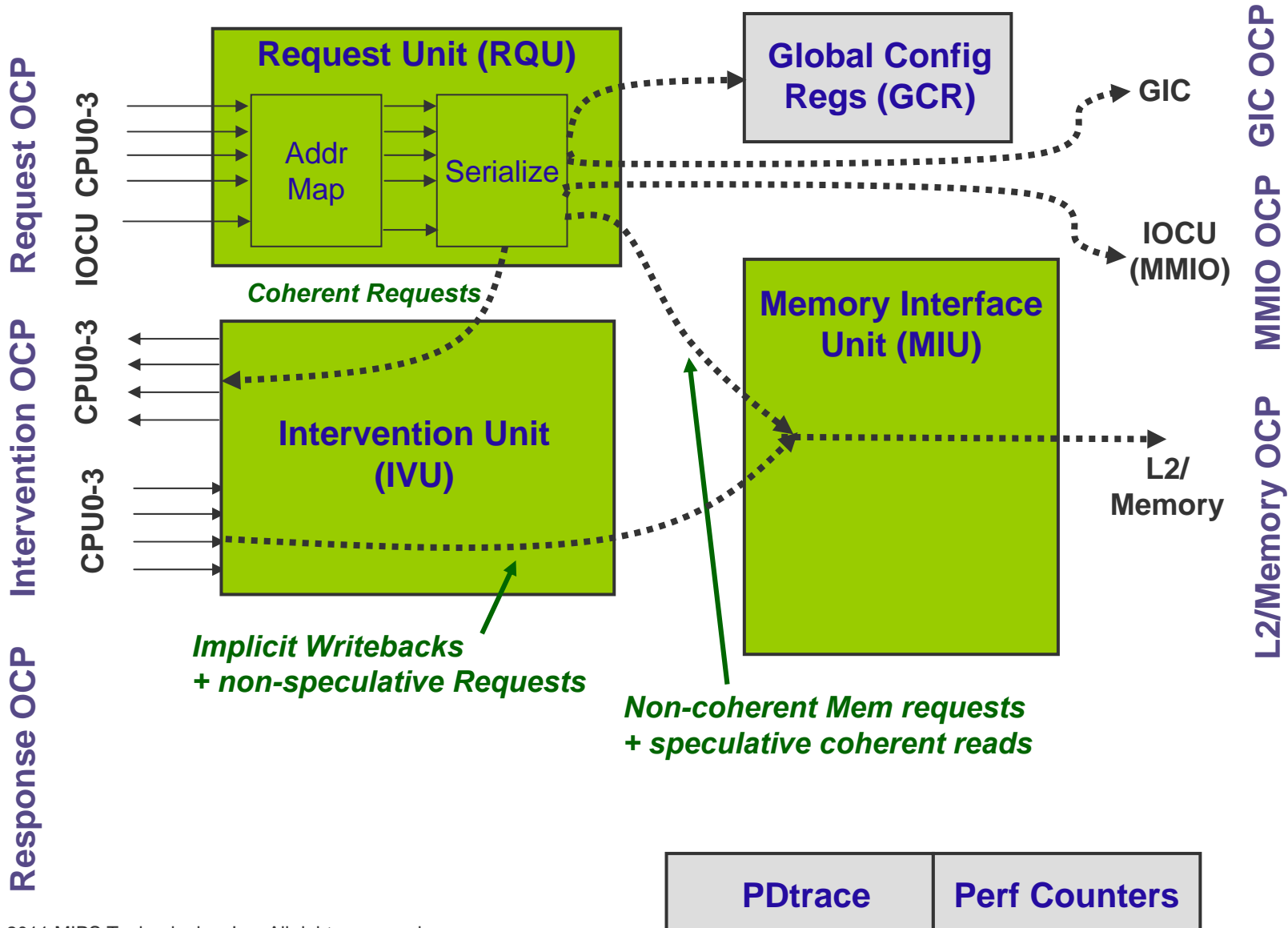
At the core of the user experience.®



# 1074K Coherence Manager (CM)

## High-Level Request Flow

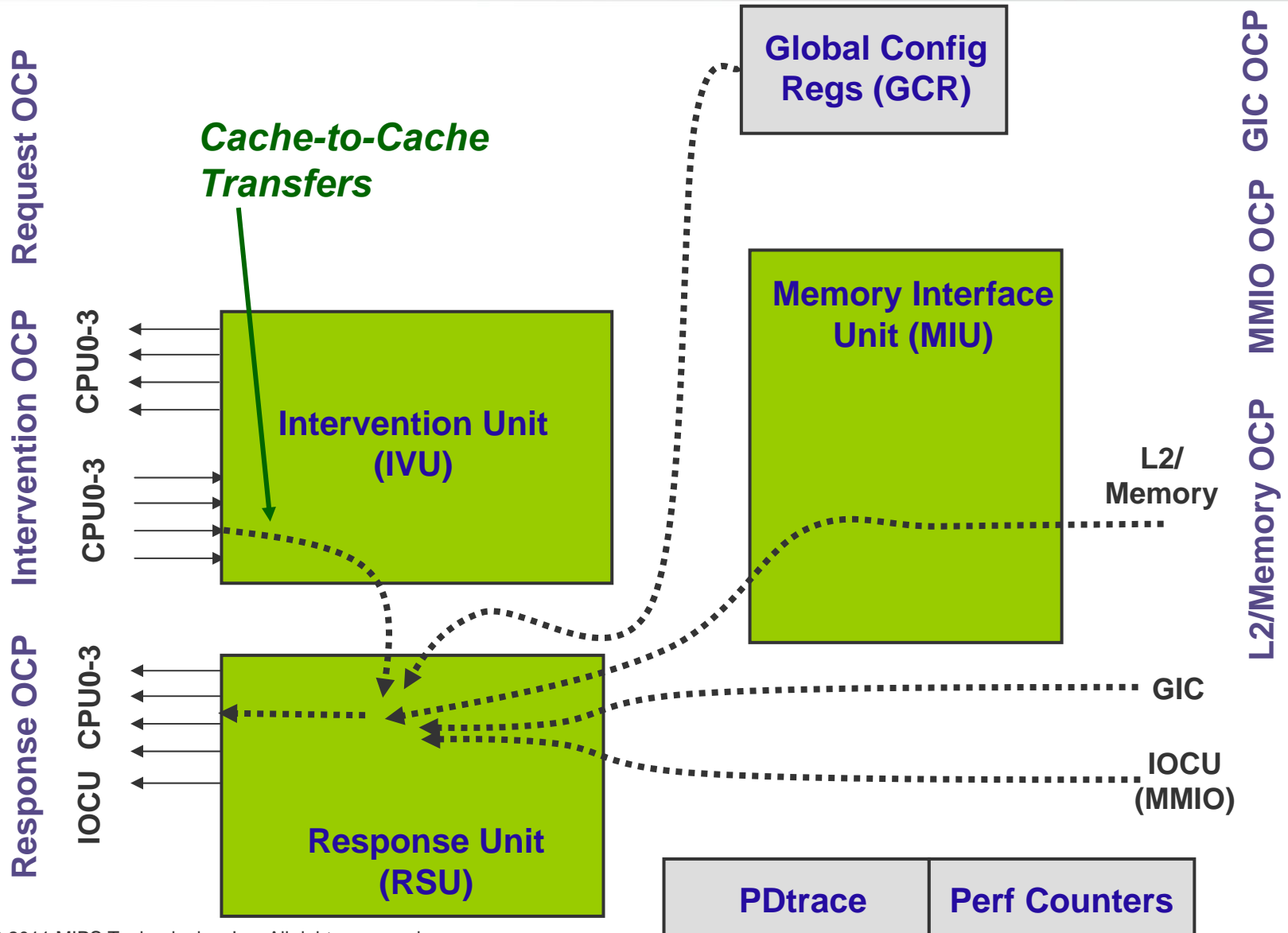
At the core of the user experience.®



# 1074K Coherence Manager (CM)

## High-Level Response Flow

At the core of the user experience.®



# Coherence Management Peripherals

## ❖ Global Interrupt Controller

- Provides multicore system-level interrupt control and distribution
- Interrupt routing to specific processor in the cluster
- Inter-processor interrupts

## ❖ I/O Coherence Unit

- Provides cache coherence on I/O Read/Writes without software overhead
- Transactions may be coherent (L1), non-coherent cached (L2), or uncached (direct to memory)

## ❖ Cluster Power Controller

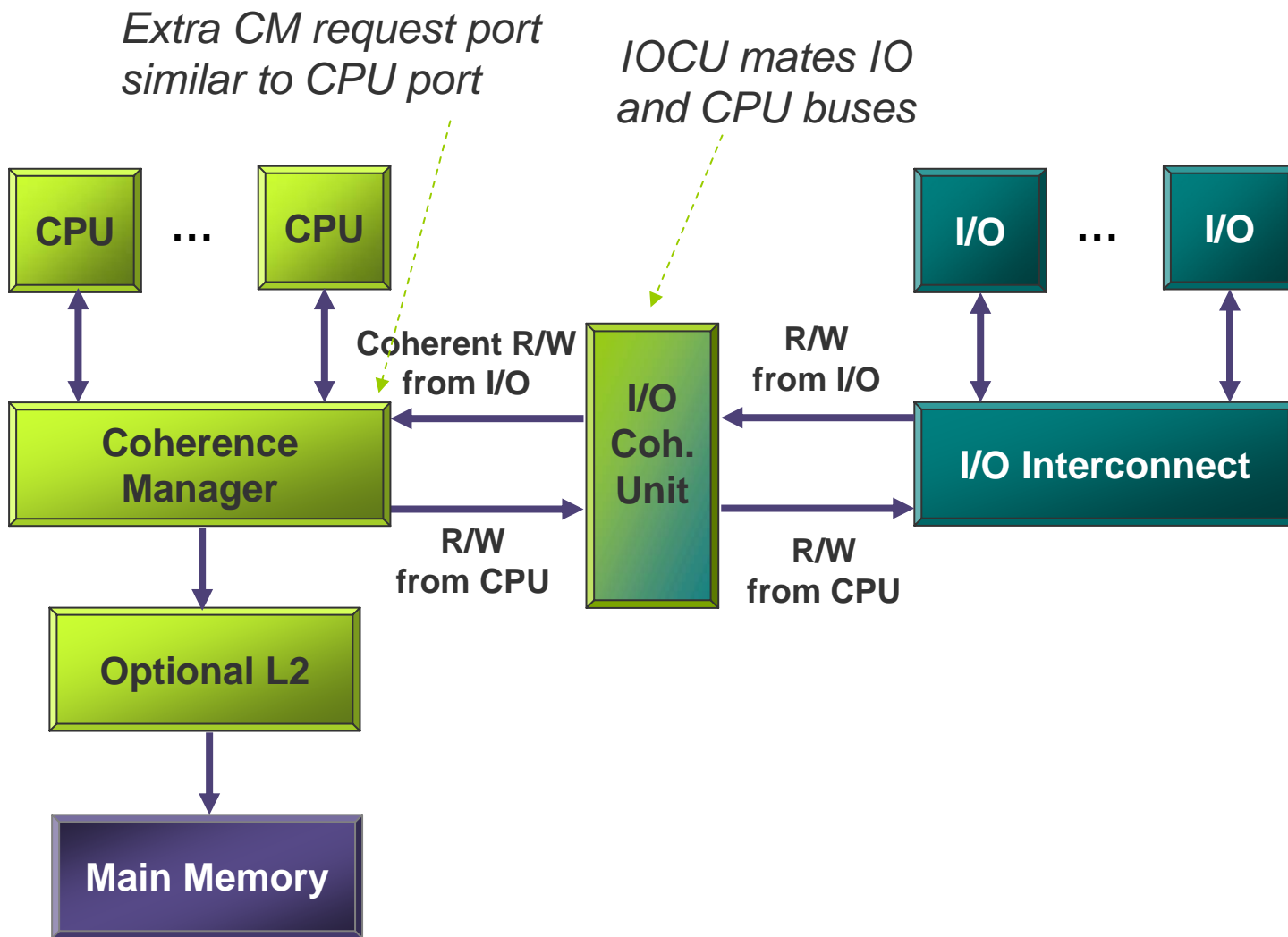
- Provides cluster-wide power gating, clock and reset control
- Register-based programmable peripheral, accessible through OS
- Wake-up scheduling through external events or peer CPU access

## ❖ PDtrace™ Debug Logic

- Provides aggregated trace access to cores and coherence management elements in the 1074K CPS

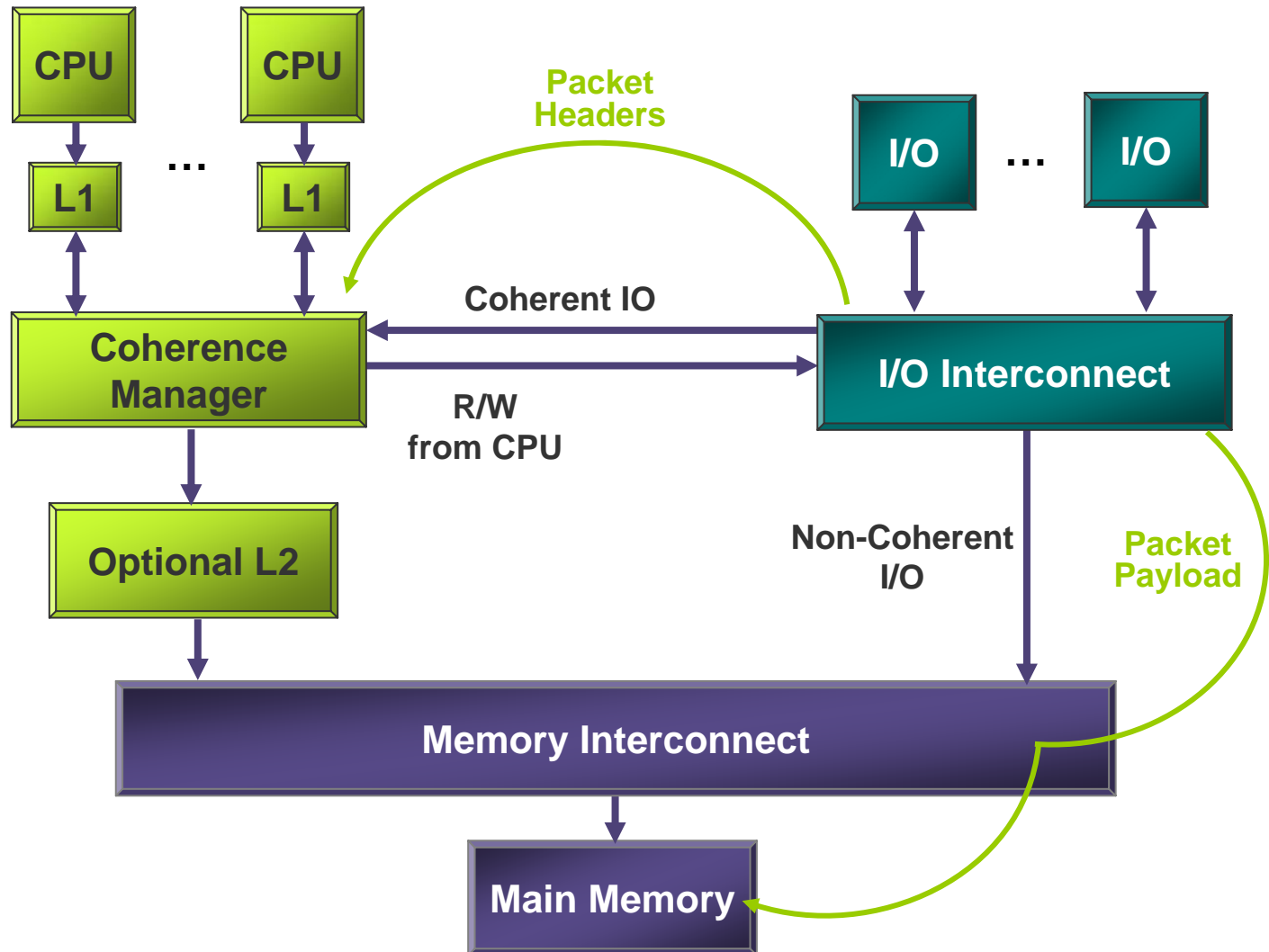
# HW IO Coherence

At the core of the user experience.®



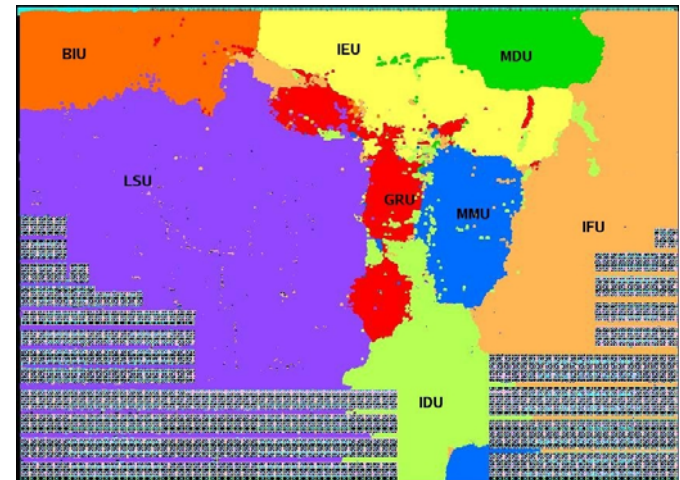
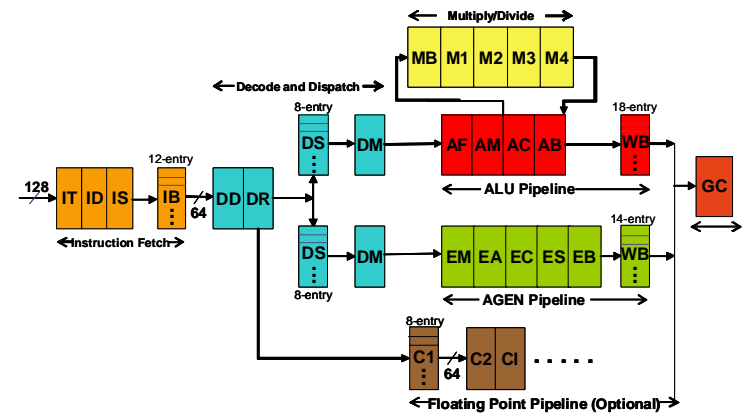
# Hybrid HW / SW IOC

At the core of the user experience.®



# Base 1074K Core Features

- ❖ **Dual-issue integer pipeline, feeds two execution pipes**
  - AGEN: load, store, branch, jump
  - ALU: the rest
- ❖ **Optional dual issue FPU, in parallel**
- ❖ **Out-of-order dispatch over a 16 instruction window**
- ❖ **Enhanced branch prediction**
  - Majority voting across 3 tables
  - JR cache predicts register indirect jump targets
- ❖ **Hardware instruction cache prefetching**
  - Software configurable prefetch of 0, 1 or 2 cache lines
- ❖ **Non-blocking data cache**
  - Supports 8 cache line misses, and 9 load misses
- ❖ **Scratchpad RAM support**

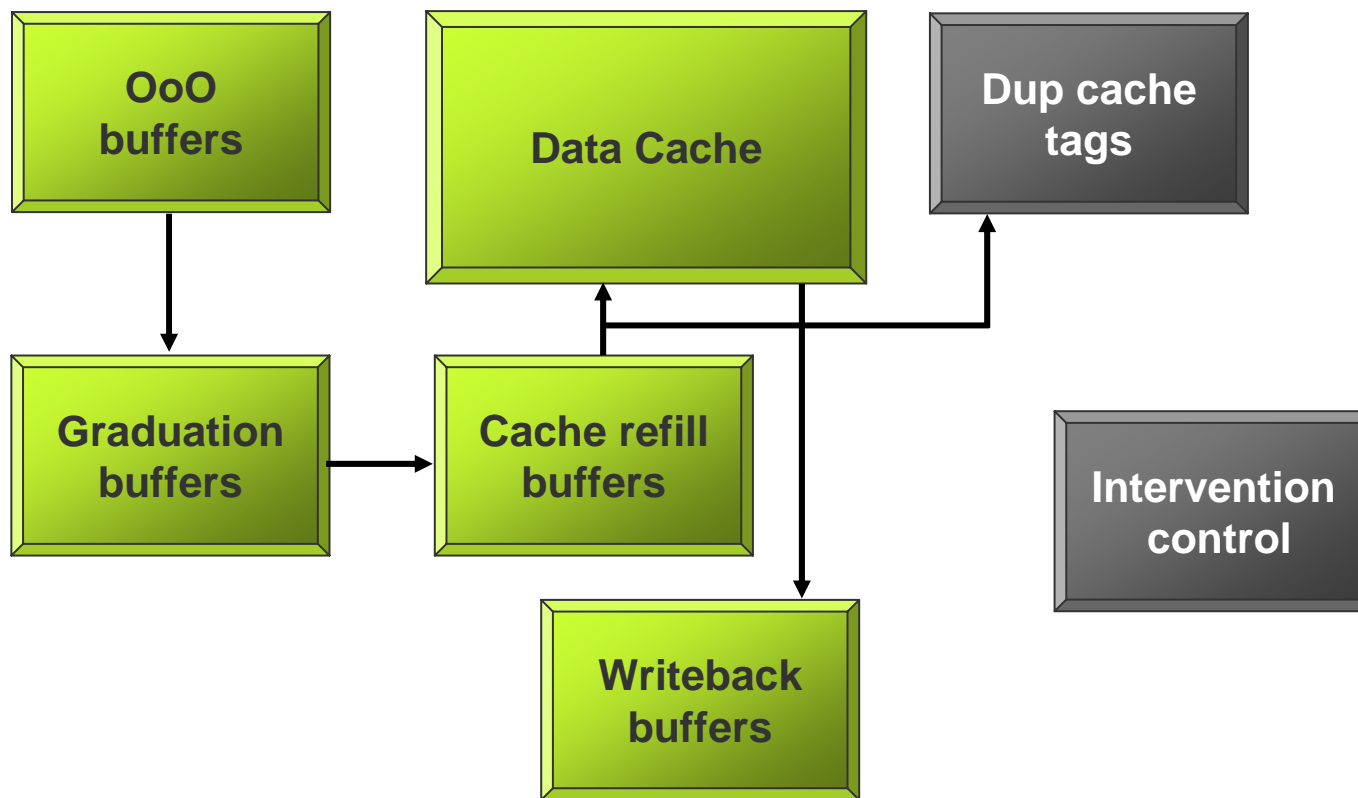


Highly configurable architecture – flexibility of soft IP

# Fast Data Transfer within Each Core

- ❖ **128-bit wide data cache interface**
  - Compared to the traditional 32- or 64-bit interface
  - Allows cache line fills and evictions to happen in 2 cycles
- ❖ **Overlapped data cache access**
  - Acts as multi-ported data cache in the presence of many writes
- ❖ **Efficient cache arbitration, reduces overhead between transactions**
- ❖ **Optimized block memory operations**
  - Prefetch hides read memory latency
  - “Prepare for store” provides low overhead zeroing of data

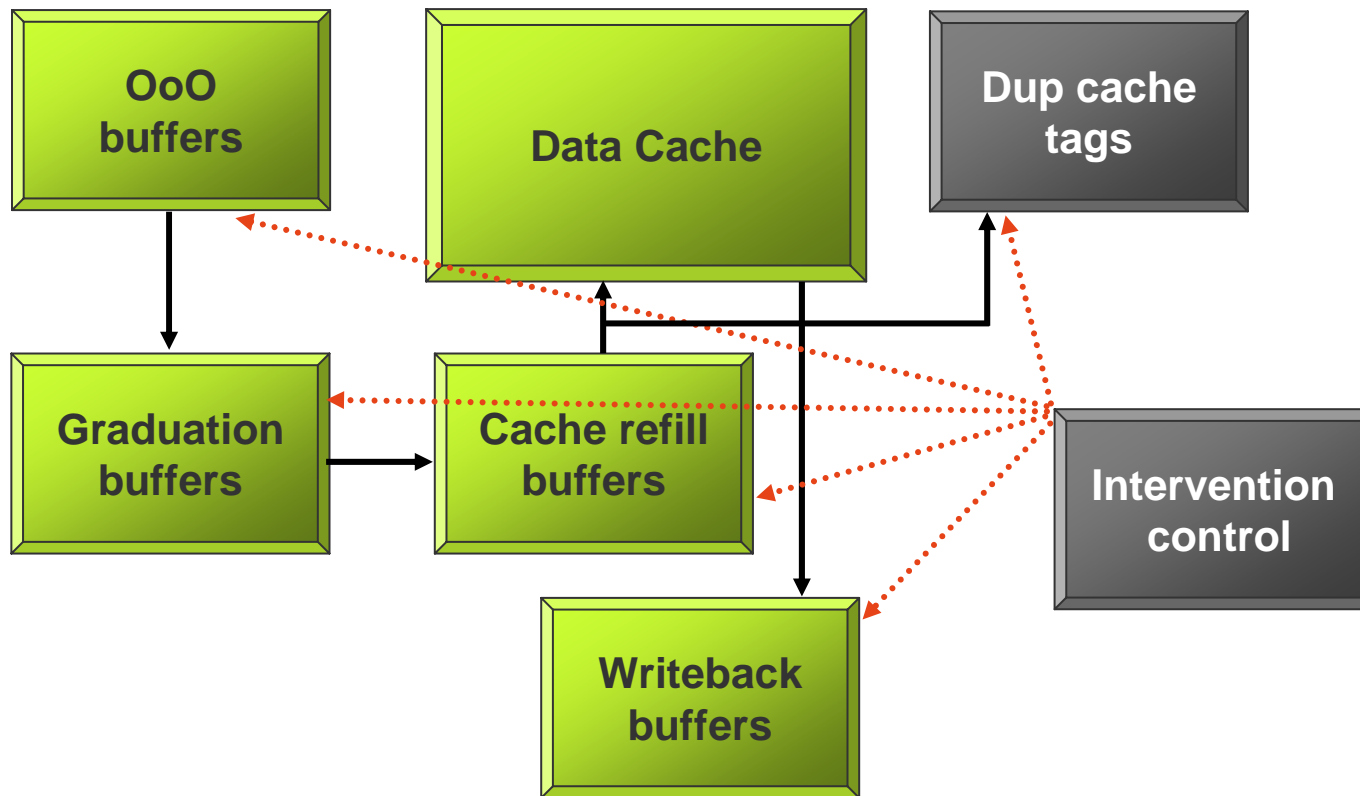
# Coherence at High Speed



## ❖ Fast intervention response

- Split “state” and “data” responses
- Duplicate tag lookup provides “state” response

# Coherence at High Speed



## ❖ Aggressive address checking and state tracking

- Allows main pipeline and interventions to proceed with minimal interference
- Handles data consistency efficiently

# Summary

*Builds on decades of multiprocessing experience –  
A new performance point for MIPS soft IP*

*Balanced, cache coherent design delivers high  
throughput from CPUs to memory system*

*High performance CPU with CMP enables scalability  
in home/wireless networking applications*

*Available now; multiple licensees  
[www.mips.com](http://www.mips.com) for more information*



At the core of the user experience®

**Thank You!**

MIPS, MIPS32, MIPS64, MIPS-Based, MIPS-Verified, MIPS Technologies logo are trademarks of MIPS Technologies, Inc. and registered in the U.S. Patent and Trademark Office. MIPS, MIPS32, MIPS64, MIPS-Based, MIPS Logo, MIPS Technologies Logo, CorExtend, Pro Series, microMIPS, M14K, M4K, 4KE, 4KEc, 24K, 24KE, 34K, 74K, 1004K, 1074K, MIPS Navigator, and FS2 are trademarks or registered trademarks of MIPS Technologies, Inc. in the United States and other countries.