

OCP-IP News

Partner Update: GSA's Semiconductor Ecosystem Summit



Global Semiconductor Alliance

GSA's Semiconductor Ecosystem Summit, on October 6th, is an executive conference focused on three

core components of the semiconductor business model - supply chain practices, technology evolution, and financial trends. Critical topics being addressed include collaboration in the mobile ecosystem, supply chain practices for sustainable partnerships, smart technology development, hardware/software integration and redefining the funding model, to name a few.

GSA is excited to offer conference attendees a unique experience before the VIP dinner when Dr. Aart de Geus, Chairman and CEO of Synopsys, interviews Scott McGregor, President and CEO of Broadcom. In this conversational interview, de Geus will ask McGregor to provide insights on some of the lessons learned as he led his company in a constantly changing environment and the role that collaboration played in this accomplishment. In closing, these dynamic leaders will provide their reflections on the day's program and address specific issues that were highlighted during the event.

Conference speakers include:

- Tudor Brown, President, Arm
- Dr. Aart de Geus, Chairman & CEO, Synopsys

- Len Jelinek, Director & Chief Analyst, Semiconductor Manufacturing, IHS iSuppli
- Scott McGregor, President & CEO, Broadcom
- Sanjay Mehrotra, President & CEO, SanDisk Corporation
- Dan Niles, Co-Chief Investment Officer, Alpha One Capital Partners

GSA is offering a special promo code worth \$100 off registration fees, so sign up today! Visit www.gsaecosystemsummit.com and use promo code (vip2011) when registering. Contact Nicole Bowman for more details at nbowman@gsaglobal.org or 972.866.7579 ext. 129.



EVE, a leader in hardware/software co-verification, has joined OCP-IP as a Sponsor-Level Member. EVE products shorten the overall verification cycle of complex integrated circuits and electronic systems designs. Its products can be integrated with transaction-level ESL tools and software debuggers, target hardware systems, as well as Verilog, SystemVerilog and VHDL simulators. www.eve-team.com

President's Overview



Ian Mackintosh
OCP-IP Chairman and President

Welcome to this edition of the OCP-IP newsletter.

As we bring summer to a close and head into cooler weather and the colors of Fall we are pleased to see the many deliverables that will be completed and available to our members by the end of the year.

Our goal at OCP-IP is always to create an organization with the tools and infrastructure necessary for our members to quickly and easily leverage the benefits of the OCP specification.

With that goal in mind, the OCP-IP Specification Working Group is busy completing OCP 3.1 which will include work by the Functional Verification Working Group on compliance properties for the 3.0 Coherence extensions and the IP-XACT schema created by the Metadata Working Group.

Our NoC Benchmarking Working Group will shortly announce the availability of an enhanced version of their Transaction Generator. The new version will now include the Accurate Dynamic Random-Access Memory Model (ADM) package, and adds nine new models. The current version of the package is now freely available during to both OCP-IP members and non-members alike, through GNU LGPL licensing at http://www.ocpip.org/tg_package.php. In addition, the NoC BWG has also been collecting new paper submissions for an update to the OCP-IP Research Bibliography. The OCP-IP bibliography is an innovative tool that allows students and researchers to quickly and easily locate critical research documents and papers in the field of on-chip communication for use in studies and research projects.

Everyone is welcome to submit

references for inclusion in the next update through our online submission tool available by clicking [here](#).

OCP-IP now offers an all new "Introductory Presentation." This new presentation contains audio files which more fully explain each slide. A copy of the new Introductory presentation is available [here](#).

Our Marketing Working Group is hard at work preparing for the OCP Forum in Shanghai scheduled for Oct 25th. Please see page 7 for all the exciting details surrounding this event. Lastly, the marketing team has updated our "OCP-Inside" presentation. To see just a small sample of the many leading edge products featuring OCP, please see our newly updated "[OCP Inside Presentation](#)."

For a full update on the activities of all working groups, please see page 5 of this newsletter.

Sincerely,
Ian R. Mackintosh
Chairman and President, OCP-IP

New Member Spotlight

VISENGI is an IP design firm based in Spain and specialized in high speed video coding and



cryptography
HW IP cores,
as well as
EDA SW for
source code
obfuscation.

Building on an extensive knowledge and experience, VISENGI currently supplies its products and design services to important firms in several continents. www.visengi.com

What Debug and Medicine Have in Common

By Albrecht Mayer OCP-IP Debug Group

Courtesy Electronic Design Magazine

Healthy people don't need a doctor. But there's an old physician's joke stating that there are no healthy people—just those who haven't yet been examined. By analog, viewing Debug from the critical business perspective, one must ask: How much examination time and critical resources should be spent searching for critical problems early on in the design process?

The human body has tremendous complexity. Similarly, today's embedded systems have reached a complexity level that's far beyond simple proof of correctness by any mathematical or formal method. It's also clear that there are great similarities between medicine and debug. This article takes a closer look at both the similarities and differences between medicine and debug. It also examines the "best practices" leveraged in medicine that could be adopted into the debugging of systems.

First, consider the case wherein being one mile away from a cliff's edge is quite safe. However, the situation of being one step away from that same edge can be very dangerous. In fact, it could soon cause an ambulance to be sent on its way. The same can be said in debugging systems. How far away from the edge of disaster are you in debugging your system?

Medicine normally comes into play only after we fall off the cliff. The same is often true for debug. In this example, it's obvious that there's a danger zone close to the cliff. Similarly, the solution to the problem is very obvious: Don't go

near the cliff. In other examples (such as debugging systems), the root cause of failure and preventative measures that should have been taken aren't always as obvious.

When problems are obscure, identifying them can take time. Because debugging is typically in the critical path, there isn't always time for a deeper look. However, all forward-thinking companies will spend at least some effort (no matter how small) recording bugs. This allows for classification and statistics to identify hot spots and troubling issues. It makes sense to spend effort taking these preventative measures early in the process.

DEADLY RISKS AND DISEASES MAY NOT HAVE A SYMPTOM

Discovering deadly risks and diseases by statistics alone may not be the best or safest option. For safety—particularly in critical embedded systems—all

bugs need to be found before a product is deployed in the field. In the previous cliff example, the risk is visible to all, except the blind. In the area of embedded systems, the fraction of blind chips (those chips with no adequate on-chip observation capabilities) is a significantly higher percentage than that of the physically blind in the human population.

Even if a chip contains observation capability,, somebody still has to take the time to look at and analyze the data. The problem is that risks are usually not as obvious as they are in the cliff example. Again, as systems are so



complex, there are many spots that need to be reviewed—in fact, too many for all of them to be reviewed. To get a better idea of how to address this problem systemically, we can look at how similarly complex problems are addressed in medicine.

In a physical exam for instance, many different blood tests are taken and the results are measured. This is a highly automated process. For each of the results, a range is given. The doctor only needs to look at the values that are out of the “normal” range. For some values, there may not even be an absolute range. The value of the information sometimes lies in the trend of the number over time.

We can take a similar approach for embedded systems with standardized measurement values. These value statistics could be instance (i.e., average, maximum, and minimum) of general system properties, such as cache misses, hits, bus conflicts, interrupt latencies, CPU idle time, task deadline distances, etc. These general values can be measured without any knowledge of the specific system. The same can be done for system-specific critical parameters.

Like measuring the electrocardiogram (ECG) under stress, this standardized value measurement can be done (say) with an additional artificial task or interrupt load. The stress can then be increased until we find the first functional issue. If this additional stress-load is very small, you’ll know that you’re close to the cliff.

PROBLEMS ARE MORE THAN THE OBVIOUS BROKEN LEG.

Medicine deals with both very obvious problems, such as a broken leg, and obscure diseases that are little known. In the past, debugging was very simple (like fixing a broken leg) compared to the challenges faced today. Then, simply finding the line of C or assembler code and banging your head against the monitor would provide a fix. This class of bug still exists. In addition, there are now many

issues that can’t be detected by simply single-stepping over some suspect code.

There’s a new class of system bug or issue, which is more closely linked to data values and execution delays than to program flow. A troubling property of such a system issue is that there’s frequently no digital rule for right or wrong data, as there is for a classical bug. Sometimes, the observation of such an issue will even challenge the specification of the system. Of such issues, the first type is the possibility that the algorithm is correct, but calculation deadlines sometimes can’t be met (due to different kinds of complex overload situations of critical system resources). In a second type, the algorithm itself results in a wrong control output for certain input-value scenarios.

From a debug perspective, there needs to be a diagram created over time with the relevant data for both types. For the first type, these are the load situations of the critical resource in relation to the control algorithm. For the second type, the observation of the control algorithm—with all relevant input, intermediate, and output signals—is sufficient. Such a diagram is then analyzed by a human expert or system-specific tool.

The main requirement for the chip is the capability of observing the data values (signals) consistently and in parallel. Program flow trace is of much less importance.



To read the full text of “What Debug and Medicine Have in Common” please visit [Chip Design Magazine by clicking here](#)

Albrecht Mayer is Senior Principal Engineer for Emulation Systems and Tooling at Infineon. Within the microcontroller business unit

he is responsible for on-chip debug architectures and C-modeling methodology. He has published many papers and holds more than 20 patents in these areas. He represents Infineon in the OCP-IP (www.ocpip.org) Debug Working Group activities. Dr. Mayer received his Diploma and PhD degrees in electrical engineering from the Technical University of Munich

Working Group Updates

Debug Working Group:

The Debug Working Group is actively disseminating the standard framework at conferences and is open for calls to collaborate on a standard debug block at either an ESL or RTL level. The Group is also working on additions to the debug interface 3.0 including cache coherence and power management features for SMP, AMP, multi-threaded, and other system architectures. The Group has set a goal for an OCP 3.0 compatible debug systems white paper to be published along with an updated debug specification supporting OCP 3.0 to be available by EOY 2011. Finally, the group is additionally collaborating on a Debug focused chapter for a new OCP-focused book.

Metadata Working Group:

The Metadata Working Group (MDWG), released a package of metadata vendor extensions in 2010 . These extensions are enhancements created to fully capture configurable interfaces (such as OCP) using the IP-XACT format defined by the Accellera Consortium. The package is both IPXACT 1.4 and IEEE1685 compatible and has configuration checkers for OCP2.2. The MDWG continues to develop the OCP3.0 package which includes bus definition, abstraction definition & configuration checkers for OCP3.0 . This package will be released in 2H11. For more information on the metadata vendor extension package please see our data sheet available at:

www.ocpip.org/datasheets.php

System Level Design Working Group:

The SLD Working Group maintains three download packages: the base OCP Modeling Kit (OMK), the extension package for the OMK including monitor and abstraction-level-adapter components, and the example virtual platform (VP) which demonstrates use of the OMK. A new release of the OMK and monitor package is currently being prepared which expands coverage to more of the OCP protocol, adds more adapters, and addresses a few issues discovered by users. The new adapters are native TLM-2.0 and enable efficient connection of loosely-timed, approximately-timed, cycle-accurate and RTL models. Subsequent work in the SLD Working Group will ensure the continued compatibility of the OMK with the latest versions of SystemC and TLM-2.0 available from OSCI and major EDA vendors, and collaboration with the Metadata Working Group on use of IP-XACT to automate system-level-design activity with OCP components.

Specification Working Group:

The Specification Working Group is continuing work on OCP 3.1, which will include extensions in the area of memory semantics to support weakly ordered memory systems and in the area of performance parameters that describe available IP core concurrency which in turn helps system integrators optimize performance while minimizing hardware costs. In addition, OCP 3.1 will also include work by the FVWG on compliance properties for the 3.0 Coherence extensions and the IP-XACT schema created by the MDWG.

NoC Benchmarking Working:

The NoC Benchmarking Working Group recently released an Accurate Dynamic Random- Access Memory Model (ADM) package and is now integrating the DRAM into Transaction Generator tool. This allows modeling shared memory communication in addition to message-passing. The WG is currently finalizing the new TG release which will also include a set of 9 traffic models. The package will be freely available during the fall to both OCP-IP members and non-members alike, through GNU LGPL licensing.

An existing version of the package is already freely available to both OCP-IP members and non-members alike, through GNU LGPL licensing at http://www.ocpip.org/memory_model.php.

Functional Verification Working Group:

The Functional Verification WG has completed targeting the definition of the functional verification checks and coverage to support OCP 3.0. They have completed the work focused on Cache Coherence Extensions, specifically targeting configuration checks, signal checks and transaction-level checks. The final set of verification documents is expected to be released in 4Q11.

Marketing Working Group

The MWG is busy preparing for the OCP-IP Forum in Shanghai, China in late October. In addition the Group has also updated the "OCP Inside" presentation. Finally, the group continues helping member companies compose and place their OCP-related articles and conference papers, while supporting the ongoing publication of the OCP-IP newsletter and our various press releases.



Protocol transducers play an important role in incorporating existing designs into an SoC. Automatic transducer

synthesis from formal descriptions of protocols is effective, since it can generate a customized transducer for each incompatibility. Previously VDEC developed a synthesizer, called STEP, which automatically generates protocol transducers from FSM specifications for two independent protocols. Modern on-chip bus protocols, however, have incorporated complicated mechanisms in transactions to achieve higher performance by decreasing communication latency and bus occupancy. Those mechanisms make it difficult to synthesize the transducer automatically, as well as describe specifications of protocols. Despite the progress of the latest studies, it is still difficult to synthesize protocol transducers that can handle burst transactions from modern practical protocols concisely and without limitations. In burst transaction, total count of iteration of data transfer is given with a data word at the beginning of a transaction. It is impossible for existing synthesis methods to handle iterative transfers whose maximum iteration is given with data words, because of the limitations in formal definitions for protocols. Some synthesis methods, with extended specification of target protocols, can handle the iterative transfers. They, however, have significant limitations in handling data words.

In existing synthesis methods, transducers pay almost no attention to the values of the data words. Transducers take a data word from a channel and simply pass it into the other channel. This is caused by the lack of formal descriptions on the semantics of data words in the specifications of protocols. By contrast, the data words can represent protocol-specific information such as addressing mode (linear or modulo), length of iteration, tags of multithread operation and error codes. In addition, the data words can have protocol specific definitions of encoding rules such as range of possible values, bit width, bit-encodings (linear, power of two, gray

code) and enumeration tables. Because of the lack of information, it is difficult for the resulting transducers to realize the state transitions depending on the value of data words. Also, there can be a mismatch of encoding rules for the same kind of data channels between two protocols.

VDEC has developed an enhanced version of STEP which can resolve the problems noted above. The method consists of two novel ideas. The first one is incorporating datapaths into transducers. Additional datapaths can fix semantic mismatches on data words between two protocols, and realize appropriate behaviors depending on the value of data words. The second solution is a FSM synthesis method that can take more than two FSMs at a time. FSMs generated from this synthesis method can connect the master, slave and the additional datapaths, with minimized latency in terms of cycle counts, to finish a transaction that is common in modern protocols. For an application of the two ideas, VDEC developed new architectures and synthesis flows of transducers for burst transactions. We then carried out an experiment to show that the proposed method can handle burst transactions from modern real-life protocols, such as full set of OCP. The results also showed that the size of the resulting transducer is much smaller than a transducer from existing methods.

Prof. Fujita received his Ph.D. from the University of Tokyo in 1985. He is a Professor in VLSI Design and Education Center (VDEC) at the University of Tokyo. Prior to joining the University of Tokyo in 2000, he was Director of CAD in Fujitsu Laboratories of America for 6 years. He has done innovative work in the areas of digital design verification, synthesis, and testing. He has co-authored 6 books, and has over 150 publications. He has participated and chaired many prestigious conferences in CAD and VLSI designs. His current research interests include synthesis and verification in higher level design stages, hardware/software and digital/analog co-design.

The 2011 OCP Forum in Shanghai China is being organized by our friends at SSIPEX and will be held at the Oriental Riverside Hotel of the Shanghai International Convention Center on Oct 25th 2011.

The OCP Forum will focus on the issue of SoC Design. Speakers are from established leading companies with mature, proven, and leading-edge products. The entire span of design will be considered including facilities that aid rapid design, ensured IP reuse, efficient assembly and world-class verification.

Speakers include:

- Ian Mackintosh, OCP-IP
- David Zhang, Cadence
- Howard Pakosh, Chipstart
- Lauro Rizzati, EVE
- James McHale, Sonics
- Chunlin Zhang, Synopsys



Presentations from the event will be available at http://www.ocpip.org/papers_and_presentations.php on Oct 25th

Who should attend:

- System and Semiconductor design companies
- SoC design and verification engineers including system and chip architects
- Engineering decision makers from Senior Engineers to VPs
- Business decision makers including CEOs



Functional Checks and Assertions Now Available to Sponsor-Level Members!

The latest comprehensive set of Functional Checks and Assertions is available now to Sponsor-Level Members. Compliance checks eliminate the need for “best-guess” verification by engineers, making certain an OCP interface complies with the specification, assuring verification quality and that IP blocks are compatible at the system level. This current set of checks supports OCP 3.0 and is now being extended for the next release of OCP, already in advanced stages of development. For your copy contact admin@ocpip.org

All Now Available!

OCP Virtual Platform (VP)

The VP is a loosely-timed model of a simple embedded platform which runs the Linux operating system. Some of the memory-mapped peripherals are modeled using the OCP Modeling Kit (OMK), further demonstrating the use of the kit. To obtain an overview and basic understanding of the Virtual Platform, please refer to our [Datasheet](#). To download a free copy of the VP, click [here](#).

Transaction Generator

The Transaction Generator (TG), is a transaction level (TL) SystemC simulator for benchmarking Network-on-Chips (NoCs) used in multiprocessor system-on-chip (SoC) applications. Utilizing this tool makes simulation of larger systems substantially faster and results obtained at this higher level can be accurately used as an initial estimate in selecting and fine-tuning NoCs. The tool is freely available through the GNU LGPL. For your copy click [here](#)

OCP Tracker

Is a software tool that provides graphical performance, statistical and transaction analysis of OCP interfaces and fabrics. It also enables validation of performance metrics via a built-in regression manager. OCP Tracker seamlessly interfaces with OCP-IP's [CoreCreator II](#) trace files to allow bandwidth, latency and other types of performance metrics to be analyzed. To request your copy of Tracker click [here](#).

IEEE 1685 Vendor Extensions

Vendor Extensions provide a way to fully describe configurable interfaces, (such as OCP) in machine-readable XML structure in an IEEE standard format. They are compatible with both IP XACT 1.4 and [IEEE1685](#). The package is available to both OCP-IP members and non-members alike. Members may access the OCP Metadata Vendor Extension package by completing the online click-through [Commercial Metadata Vendor Extension License](#). Non-Members may access the package via online click-through [research license](#).

OCP 3.0 Specification

The Specification Working Group formally released the OCP 3.0 Specification in November, 2009. This latest version contains extensions to support cache coherence and more aggressive power management, as well as an additional high-speed consensus profile and other new elements. For a copy complete our [Research License Agreement](#).

OCP Checker Now Part of CoreCreator II

The OCP checker is a fourth-generation solution for validating protocol compliance of master and slave devices using OCP. It is based on SystemVerilog Assertions (SVA) and can be used with all major logic simulators. It supports the complete set of protocol compliance checks defined in the OCP specification and spans the full range of OCP socket configuration options. The OCP checker can also generate trace files in the standard ".ocp" format for post-processing. It can be obtained, as part of CoreCreator II [here](#). For a free copy members can contact admin@ocpip.org

Debug Specification Version 1.0

The specification provides guidelines and recommended signal interfaces for on-chip debug of OCP-based systems and related multicore architectures. It describes a debug socket as a framework for IP and tools providers to develop comprehensive and re-usable debug and instrumentation environments that provide on-chip analysis and control features. These include trace, triggering, multicore synchronization, etc., along with recommendations for integration within ESL environments. For a copy of the spec click [here](#).

NoC Benchmarking Specification, Part 2 of 2

The specification presents a generic NoC architecture, a comprehensive set of synthetic workloads as micro-benchmarks, workload scenarios and evaluation criteria. These micro-benchmarks enable you to measure and pinpoint particular properties of NoC architectures, complementing application benchmarks. Click [here](#) for a copy of the spec.

NoC Benchmarking Specification, Part 1 of 2

The specification presents a modeling methodology for applications running on multicore systems and it defines an XML format for documenting and distributing NoC benchmarks. It defines a black-box view of the processing elements that discloses only the relevant computational aspects for interacting with the on-chip data transport mechanism. Click [here](#) for a copy of the spec.

OCP SystemC TLM Kits

The new kit is the first, and most advanced TLM2-based, industry-ready kit in existence today. The kits significantly increase performance, ease-of-use and ensure alignment with the OSCI 2.0.1 standard. Kits are free as part of OCP-IP membership. Non-Members may obtain a free research version. For more information contact admin@ocpip.org

Transaction Analysis Tool

The OCP Conductor Tool is an innovative, detailed OCP transaction viewer that enables fine-grained analysis of bus transactions. A complete transaction sequence can be traced from request to response, along with a host of related information about the transaction. For a free copy contact admin@ocpip.org