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OCP-IP News

OCP-IP Partner News: Accellera Continues Growth, Develops New Standards

Accellera, an industry organization formed in 2000, provides design and verification standards for quick availability and use in the electronics industry. It completed its merger with The SPIRIT Consortium in April 2010 and added several new members, including NXP and ST to its Board of Directors. The Board of Directors elected Dr. Shishpal Rawat of Intel as the Chair of Accellera.

The new organization and its members cooperatively deliver much needed EDA and IP standards that lower the cost to design commercial IC and EDA products. Two of the most active and visible activities are focused on creating a Universal Verification Methodology (UVM) and continued enhancement of IP-XACT.

New Member Spotlight

Truechip Founded in 2008 and based in the New Delhi Area of India, Truechip is a privately held company with a team of employees focused on IP Design and Design Services. The company specializes in Low Power Sign-off, VLSI Design Services, ASIC Design Services, both front end and backend design services, and IP Design. For more information on this OCP-IP member, please visit www.truechip.net

The Verification IP Technical Subcommittee (VIP-TSC) released UVM Early Adopter (UVM-EA) version in May. This was quite visible at the Design Automation Conference with more than 125 attendees at the 7:00am breakfast panel “UVM: Charting the New Territory”, sponsored by Accellera. The VIP-TSC, with active participation from users such as AMD, Cisco, Freescale and Intel, the three large EDA vendors Cadence, Mentor and Synopsys, and several individual verification experts, is working very hard towards releasing UVM 1.0 as a standard before the end of this year.

As a result of Accellera’s partnership with the IEEE, Accellera standards are transferred to the IEEE standards body for formalization and ongoing change control. In strengthening this relationship, Accellera recently funded the “Get IEEE 1685” project, which enables the user community to download an electronic version of the IEEE 1685 (IPXACT) standard at no charge. This helps the user community to rapidly adopt the IP-XACT standard and the vendor community to build tools to support and facilitate the use of the standard.

Accellera is hosting its annual DVCon conference (www.dvcon.com) starting February 28, 2011 in San Jose where more than 600 verification engineers gather to learn about the latest advances in verification technologies.

For more information about Accellera, please visit www.accellera.org. For membership information, please email membership@accellera.org.projects

By Yatin Trivedi, Member, Board of Directors, Accellera and Director of Standards and Interoperability Programs, Synopsys

President's Overview

Ian Mackintosh
OCP-IP President and Chairman

Welcome to this edition of the OCP-IP newsletter. We have been extremely busy over the last quarter further expanding our extensive infrastructure, guaranteeing best-of-breed solutions endorsed by OCP-IP for our members.

Our System Level Design Working Group (SLDWG) recently announced the availability of a Virtual Platform Demo created utilizing OCP-IP's advanced Modeling Kit. This example platform acts as a guide to OCP-IP members enabling them to quick-start their ESL activities using the OCP-IP TLM Modeling Kit, which is fully compatible with OSCI's TLM 2.0.1. The Virtual Platform Demo utilizes Open Virtual Platforms (OVP) technology. OVP was founded by Imperas to make virtual platforms more accessible and easier to use for embedded software development. To get your copy of the Virtual Platform click here

In addition, our System Level Working Group has also released OCP Tracker. OCP-Tracker is a software tool that provides graphical performance, statistical and transaction analysis of OCP interfaces and fabrics. It also enables validation of performance metrics via a built-in regression manager. OCP-Tracker seamlessly interfaces with OCP-IP's CoreCreator II trace files to allow bandwidth, latency and other types of performance metrics to be analyzed. To request your copy of Tracker click here.

In other deliverables news, our NoC Benchmarking Working Group has released the first version of their Transaction Generator (TG). The TG is a transaction level (TL) SystemC simulator for benchmarking network-on-chips (NoCs) used in multiprocessor system-on-chip (SoC) applications. Utilizing this tool makes simulation of larger systems substantially faster and the results obtained at this higher level can be accurately used as an initial estimate in selecting and fine-tuning NoCs. To download your free copy of the TG see http://www.ocpip.org/tg_package.php. In addition, the Group has been working on a memory modeling technical article, and will publish other technical information about the TG later in the year.

Our Marketing Working Group (MWG) has updated the OCP-IP Industry Association Comparison Chart or .ORG spreadsheet to reflect recent changes at Accellera. As a result of this recent update we have recorded a large increase in viewership numbers of the .ORG spreadsheet through the summer months. In addition, the MWG has published press releases on all these new deliverables and is working on developing technical articles in their support, too. The group is also soliciting new entries for our OCP Libraries. Submitting new products or services for addition to the OCP Libraries is as simple as completing the online click-through form and is just one of the many opportunities OCP-IP members have to advertise products and services, leveraging the OCP-IP marketing team and infrastructure as part of your membership benefits. Last but not least, the MWG is helping plan for an October presentation I will be giving at JSNUG.

If you would like to contribute to future editions of this newsletter, please contact admin@ocpip.org

OCP application in vector graphics hardware IP solution
by Eisaku Ohbuchi, DMP Inc.

The SMAPH-F IP core provides a high-performance, low power vector graphics solution based on OpenVG 1.1 API, defined by the Khronos group. This IP core is integrated with an in-house based platform which has customization capabilities for various SoC implementations such as independent VRAM, embedded and unified memory architecture; this means the SMAPH-F solution can support mobile to industrial applications.

Introduction

Since the introduction of the iPhone in recent years, providing a superior user-interface with advanced graphics mechanism has become a big key in product differentiation. A highly-developed user interface in an embedded system will ensure a high quality user experience. SoC developers demand efficient and extensive graphics functions and so IP developers are confronted with difficult choices in providing graphics functions with a suitable ROI.

There are various ways to optimize the graphics functions for the user interface. For instance, a basic, primitive drawing of the line etc. is sped-up by using DSP, drawing of 2D sprite is sped-up by integrating a dedicated BitBLT module and, according to circumstances, more advanced graphics function can be achieved by introducing a 3D graphics core and while decreasing the load on the CPU. However, there are pros and cons, and these are shown together in Table. 1.

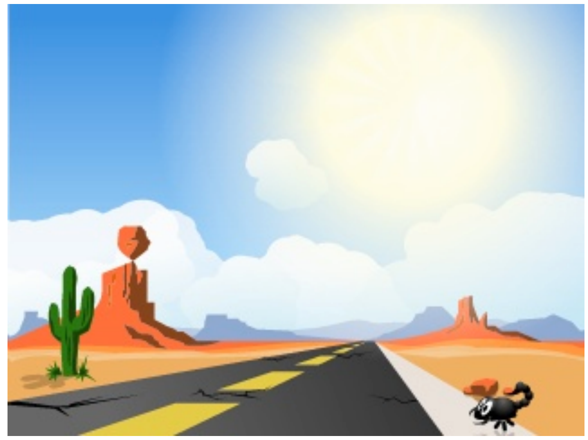


Figure 1. SMAPH-F real-time demonstration (Rightware).

The BitBLT based acceleration in 2D graphics is still considered the most reasonable cost approach when considering what is still the main current usage, the speed-up of sprite drawing. Solutions in 3D graphics have been introduced in recent SoCs; the down-side is

Table 1. Trade-off in graphics system implementation policy for user interface

Implementations	Pros	Cons
Software processing in CPU	-Can apply to an existing system.	-The demand drawing performance is not satisfied.
Acceleration of a part using DSP processing	-Can apply to an existing system in the system with the DSP core.	-When an advanced drawing function such as the texture insertion is used, the drawing performance is not enough.
Acceleration in dedicated BitBLT module	-Can apply to 2D base drawing of the Window system etc., and performance can be improved greatly.	-When a standard API is not used, portability of software is lost. -More advanced drawing processing cannot be sped-up among 2D drawing: like font drawing and Flash animation, etc.
3D graphics hardware	-Standard API such as OpenGLES is often supported and the software asset can be best utilized. -It is possible to process more advanced drawing.	-A lot of resources such as memories and CPU are needed, and the cost to obtain sufficient drawing performance is high.
Vector graphics hardware	-The cost to obtain enough drawing performance is lower than 3D graphics hardware introduction (As the image is half as complex). -The high quality and the large screen support are simple with low-cost for antialiasing. -The software asset can be best utilized by employing a standard API like OpenVG.	- It is not easy to draw for the simplest case in dense 3D though it is possible.

OCP application in vector graphics hardware IP solution (Con't)

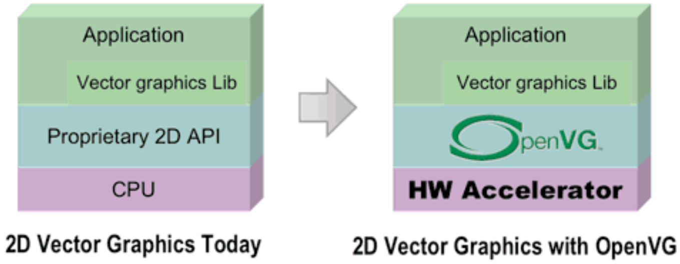


Figure 2 OpenVG API design philosophy (Source: www.khronos.org)

high cost to memory bandwidth and CPU performance, etc. to achieve viable performance.

Since the Khronos group defined Open VE, graphics hardware solutions have been announced by several companies, and this might be one solution that solves the cost-performance gap. DMP has also offers an acceleration solution for this OpenVG API with our "SMAPH-F" graphics IP core. OpenVG is an API for hardware that speeds up the vector graphics, and corresponds to an actual format such as Flash and PDF which is possible to support according to the hierarchy of vector graphics library. The system hierarchy diagram with OpenVG API is shown in Figure 2.

It is possible to offer a lower-cost, high-speed, more much higher-quality user interface with this API.

In this article, we introduce a low-cost user interface system as an example case study for our DMP SMAPH-F core.

Products overview

The outline of SMAPH-F is described below. SMAPH-F has been licensed as a vector graphics core IP supporting OpenVG1.1 for consumer equipment applications, and provides a high-speed, high-quality user interface in a low-cost system configuration. The following are key features:

- High-speed and high-quality vector graphics drawing utilizing an original, internally developed rendering algorithm.
  - Enhanced gradient functions called procedural texture (DMP original extension).
- High speed drawing for gradient animation without any memory access required for texture.
- It is possible to create a low-priced SoC by optimizing the IP core configuration selected.
- Low power consumption is achieved by operating an advanced clock gating control, according to the application requirements.
- SoC-friendly architecture:
  - Widely-used standard SoC inteconnect bus support for OCP and for AXI.
  - Effective system performance is improved by optimizing memory access to DDR burst access.
- Core size is small, so FPGA implementation is possible.

A drawing example with 50MHz operation in a FPGA demonstration system environment, is shown below. An image (Figure 5) that is an illustration used for the iPhone was implemented on OpenVG and it was possible to draw in VGA size with 30fps or more, despite an operating frequency of only 50MHz.

Hardware block diagram

This section explains architecture around the SMAPH-F memory interface. There are five masters and one slave bus around the SMAPH-F core, and these are connected to an internal bus matrix.

We addressed the following issues while developing the SMAPH-F core: 1) The IP core must support a wide range of applications from the mobile phone (with a tiny display) to an amusement-game console (with a large display) to address all embedded systems,, 2) Vector graphics hardware requires huge bandwidth for command, texture, color read/write access for large display support and this bandwidth will determine the ultimate performance of the graphics IP core, and 3) The IP core should be easy to integrate into the SoC design environment.

To comprehensively and completely address these issues, we decided to adopt OCP as the standard interface infrastructure of our building block scheme, and as a result, we can provide the following options to meet customer requirements (Table 2).

Moreover, SoC integration is readily facilitated by additionally wrapping the internal bus and offering it to the customer. SoC integration is further facilitated by the inclusions of the memory in the IP connection bus and by providing only Slave I/F x 1 and Master I/Fx1 as an

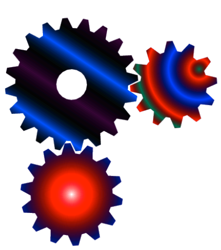
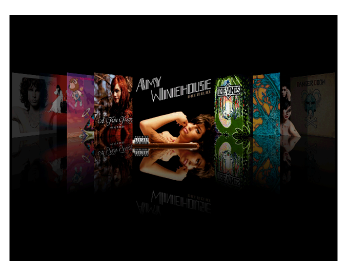


Figure 3 An OpenVG gradient rendering example

Figure 4 Procedural texture examples.



OCP application in vector graphics hardware IP solution (Con't)

IP interface implemented as wrappers, although there are two or more mastering interfaces on the inside. Performance can be also optimized by configuring the interconnect bus to ensure memory access characteristics for our graphics core.

A shared SRAM memory in an SoC can be likely to be accessed from graphics IP core, and correspondence that makes master I/F plurals can increase more than one in our platform. The graphics IP can be obtained more bandwidths, and the offer of the system that optimizes the rendering performance and access efficiency for DDR memory. It is also possible to respond to customer requirements by customizing the bridge because it is not only a standard protocol of OCP, but an additional protocol might be used within the SoC as defined by the customers' needs.

The number of multi-layers changes internally, depending on the number of slaves. Moreover, the connection to each layer is customizable for each customer.

We also support the pre-fetching mechanism using the thread protocol within OCP, and this is very important to avoid stalling the rendering pipeline and maintain high rendering performance. Table 3 shows the example of thread ID assignment in this graphics core, and in this case, the core has four texture modules.

OCP version 2.1 featured support for Tag functionality which permits out-of-order response, but this core does not support out-of-order handling, because the access for color and depth buffer needs to use read-modify-write lock- based access and the access for other doesn't have logic and FIFO for out-of-order access support to make small IP core and support wide range of application from small mobile device to the embedded system with large display. To obtain better memory access without tag function, this graphics core is optimized to block-based rasterization, where all pixel generation from triangles is done by rectangle blocks (such as 4x4), to utilize memory access by keeping long burst-length access and data access aligned with the address to obtain the good cache hit-rates for texture and color buffer.

The good news is that OCP is freely available to the public and is also supported by every major SoC vendor who develop their architectures based platform upon configurations. So, we can make some parameters in our bus interface and cache requirements based upon the OCP protocol to optimize the customer bus interface and some system characteristics per the last row of Table 1, and this provides a high level of suitable configurability for both IP provider and SoC developer.

Case study of system performance

The performance at the system level, especially within the final application, isn't always readily measurable, even though the core itself is known to produce very high performance per the specs in the catalog. To measure the system performance in the SMAPH-F core, this chapter shows an experimental performance evaluation result in a particular SoC example as a case study.

The figure below is the system configuration in this study.

Performance measurement results are shown in the following graphs. The performance of Case 1 (that operates only the GPU) is shown and other cases are normalized by Case 1 processing time. The spindle shows a number of frames, and the horizontal axis shows when Case 1 is adjusted to one show, each frame number.

See the entire article at http://chipdesignmag.com/display.php?articleId=4321

Table 2 A part of PICA200 building block options.

Component/Requirement	Parameter	Remark
Number of pixel pipeline	1-4	Depends upon required rasterizer performance and display size.
Cache and FIFO-size of texture and color buffer	(Inside parameter of 2^{nd} Tex cache and cache)	Depends upon bus access characteristics of SoC system as follows: - Read and write latency (1-50cycles) - Bitwidth for each channel (32, 64, 128, and 256 bit) - Clock frequency ratio regarding Core vs. Bus (1:1, 1:2, and 1:4) - Power control requirements (Customize option for each customer by wrapper.)

Working Group Updates

Debug Working Group:
The Debug Working Group is actively disseminating the standard framework in conferences and is open to collaborate on a standard debug block on either an ESL or RTL level.
Planned additions to the debug interface 3.0 are cache and power management features for SMP, AMP, multi-threaded, and other system architectures. Preliminary goals are for OCP 3.0 compatible debug systems white papers to be published along with an updated debug specification supporting OCP 3.0 to be available later this year.

Metadata Working Group:
The Metadata Working Group (MDWG), has released the package of metadata vendor extensions. These extensions are enhancements created to fully capture flexible interfaces (such as OCP) using the IP-XACT format defined by SPIRIT Consortium. The package is both IPXACT 1.4 and IEEE1685 compatible. The MDWG continues to create OCP configuration and interface compatibility checkers to be released later in the year. For more information on the metadata vendor extension package please see our data sheet available at: www.ocpip.org/datasheets.php

System Level Design Working Group:
The System Level Design Working Group (SLD WG) recently released a Virtual Platform (VP). The VP is a loosely-timed model of a simple embedded platform which runs the Linux operating system. Some of the memory-mapped peripherals are modeled using the OCP Modeling Kit "(OMK,") demonstrating the use of the kit. To obtain an overview and basic understanding of the Virtual Platform, please refer to our Datasheet. To download a copy of the VP, click here.

Specification Working Group:
The Specification Working Group has begun work on OCP 3.1, which is expected to include enhancements in the areas of memory semantics and performance parameters. Additionally, the Group completed an Errata document for OCP 2.2 that will apply the relevant specification clarifications from the OCP 3.0 Specification to ensure full interoperability. Members may access the Errata document here.

NoC Benchmarking Working:
The NoC BWG recently released a Transaction Generator (TG) which is now available to both members and non-members via the OCP-IP website under LGPL open source license. The TG is a transaction level (TL) SystemC simulator for benchmarking network-on-chips (NoCs) used in multiprocessor system-on-chip (SoC) applications. Utilizing this tool makes simulation of larger systems substantially faster and the results obtained at this higher level can be accurately used as an initial estimate in selecting and fine-tuning NoCs.

The Group is currently planning the second release which may include a tutorial, addition of the OCP-IP TLM Kit and a graphical user interface. To obtain a copy of the Transaction Generator click here

Marketing Working Group
The Marketing Working Group is busy preparing for an upcoming presentation at the Japan Synopsys Users Group meeting (JSNUG) in Tokyo Japan. In addition, the group continues helping member companies compose and place their OCP-related articles and conference papers, while publishing the OCP-IP newsletter. The group has recently created and published press releases regarding the IEEE 1685 Metadata Vendor Extensions, OCP Virtual Platform, Transaction Generator and OCP Tracker. If your company would like assistance placing an article, prominently targeted to the industry or directly to our OCP-IP-focused community, please contact admin@ocpip.org.

University Corner

Network-on-Chip Benchmarking Workgroup and Tampere University of Technology announce an open source simulation

Erno Salminen Ph.D
Tampere University of Technology
Department of Computer Systems

The focus of OCP-IP's Network-on-Chip (NoC) Benchmarking workgroup is to develop standardized methods and test sets for evaluating on-chip networks.

A multitude of NoCs have been proposed in academic literature, but detailed comparisons have been difficult, due to the lack of common test sets.

Tampere University of Technology (TUT), Finland.has developed a specific SystemC simulation tool, called Transaction Generator (TG). TG enables the modeling of complex multiprocessor system-on-chip (MPSoC) in terms of application workload, available computation resources, and mapping between these elements.

The evaluator provides a model of the NoC under study and connects it to terminals of the TG.

The first public release of TG is now available from the OCP-IP web site under LGPL open source license.

A second release is scheduled for 2H 2010 and will incorporate a tutorial, incorporation of the OCP-IP TLM Kit and a graphical user interface (GUI). The GUI helps designers see the trends, correlations, and anomalies in simulation statistics (CPU utilization and data rates etc.), and is therefore a valuable aid in analysis.

Copies of the TG are available to members and non-members alike under GNU LGPL

To download a copy of the TG click here

Partner News From OSCI

The Open SystemC Initiative (OSCI) recently hosted the first SystemC Japan event in Yokohama. Hundreds of enthusiastic attendees were treated to a full day of presentations from leading Japanese companies describing their use of SystemC, including Ricoh, Renesas, Primegate, and Sony, interspersed with technical updates from OSCI member companies and officers.

At a September tutorial in Grenoble co-located with PATMOS, an international workshop on power and timing modeling, optimization and simulation, an esteemed group of experts presented the motivation and unique capacities of the SystemC AMS extensions for industrial applications, with emphasis on wireless communication and automotive.

Also in September, the European SystemC User's Group held its member meeting in Southampton, shortly to be followed by its North American counterpart on Oct. 25. The North American SystemC User Group will tackle a variety of topics this year in Scottsdale, including architectural modeling, software co-design, verification, SystemC flows and methodologies, and language development for starters. Those interested in attending should visit www.nascug.org for more details.

OSCI's global event sponsors – ARM, Cadence, Forte, Mentor, Synopsys, and ExtremeDA – continue to play a vital role in bringing SystemC information to a growing and global group of SystemC devotees.

Speaking of events, look for an interesting one at DesignCon (January 2011, Santa Clara) titled "Who is the Designer of the Future?" This terrific panel will examine shifts in the role of design as ESL takes off, e.g., is the RTL designer going to move "up" to SystemC or C/C++? Is the Architect going to write code as the design? Etc.

This event will soon be featured on our video page (www.systemc.org/news/videos), along with tutorials, working group updates, and much more. Check it out for the latest and greatest on SystemC!

Now Available!

NEW! OCP Virtual Platform

The VP is a loosely-timed model of a simple embedded platform which runs the Linux operating system. Some of the memory-mapped peripherals are modeled using the OCP Modeling Kit "(OMK,") demonstrating the use of the kit. To obtain an overview and basic understanding of the Virtual Platform, please refer to our Datasheet. To download a copy, click here.

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NEW! OCP Tracker

Is a software tool that provides graphical performance, statistical and transaction analysis of OCP interfaces and fabrics. It also enables validation of performance metrics via a built-in regression manager. OCP-Tracker seamlessly interfaces with OCP-IP's CoreCreator II trace files to allow bandwidth, latency and other types of performance metrics to be analyzed. To request your copy of Tracker click here.

NEW! IEEE 1685 Vendor Extensions

Vendor Extensions provide a way to fully describe configurable interfaces, (such as OCP) in machine-readable XML structure in an IEEE standard format. They are compatible with both IP XACT 1.4 and IEEE1685. The package is available to both OCP-IP members and non-members alike. Members may access the OCP Metadata Vendor Extension package by completing the online click-through Commercial Metadata Vendor Extension License. Non-Members may access the package via online click-through research license.

OCP 3.0 Specification

The Specification Working Group released the OCP 3.0 Specification in November.2009. This latest version contains extensions to support cache coherence and more aggressive power management, as well as an additional high-speed consensus profile and other new elements. For a copy complete our Research License Agreement.

OCP Checker Now Part of CoreCreator II

The OCP checker is a fourth-generation solution for validating protocol compliance of master and slave devices using OCP. It is based on SystemVerilog assertions (SVA) and can be used with all major logic simulators. It supports the complete set of protocol compliance checks defined in the OCP specification and spans the full range of OCP socket configuration options. The OCP checker can also generate trace files in the standard ".ocp" format for post-processing. It can be obtained, as part of CoreCreator II here. For a free copy members can contact admin@ocpip.org

Debug Specification Version 1.0

Specification provides guidelines and recommended signal interfaces for on-chip debug of OCP-based systems and related multicore architectures. It describes a debug socket as a framework for IP and tools providers to develop comprehensive and re-usable debug and instrumentation environments that provide on-chip analysis and control features. These include trace, triggering, multicore synchronization, etc., along with recommendations for integration within ESL environments. For a copy of the spec click here.

NoC Benchmarking Specification, Part 2

Specification presents a generic NoC architecture, a comprehensive set of synthetic workloads as micro-benchmarks, workload scenarios and evaluation criteria. These micro-benchmarks enable you to measure and pinpoint particular properties of NoC architectures, complementing application benchmarks. For more information, click here.

NoC Benchmarking Specification, Part 1

The specification presents a modeling methodology for applications running on multicore systems and it defines an XML format for documenting and distributing NoC benchmarks. It defines a black-box view of the processing elements that discloses only the relevant computational aspects for interacting with the on-chip data transport mechanism. Download our NoC white paper for more information

OCP SystemC TLM Kits

The new kit is the first, and most advanced TLM-2.0 based, industry-ready kit in existence today. The kits significantly increase performance, ease of use and ensures alignment with the OSCI 2.0 standard. The kits are free as part of OCP-IP membership. For more information contact admin@ocpip.org

Transaction Analysis Tool

The OCP Conductor Tool is an innovative, detailed OCP transaction viewer that enables fine-grained analysis of bus transactions. A complete transaction sequence can be traced from request to response along with a host of related information about the transaction. For a free copy contact admin@ocpip.org