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**Accellera Vendor Extensions   
for IEEE 1685-2009  
  
Version 1.0**

**September 2013**

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# Overview

This section explains the scope and purpose of this standard. Furthermore, it gives an overview of the basic concepts and summarizes its contents.

## Scope

This standard describes XML schemas for IP-XACT vendor extensions that have been defined by the Accellera IP-XACT Technical Committee. These XML schemas are called Accellera Vendor Extensions.

## Purpose

This standard enables the use of the IP-XACT standard IEEE Std 1685TM-2009 in domains that are not supported by the IP-XACT standard yet. More specifically, this standard enables the use of the IP-XACT standard in analog and mixed signal flows, physical design planning flows, and power flows.

## Concepts

Accellera vendor extensions make use of accellera extension containers. An Accellera extension container is an XML element that can occur in an IP-XACT vendor extension. The containers are defined in a generic unversioned namespace to enable generic processing of standard extensions by IP-XACT enabled implementations; see Section 1.4. The sub-elements of the containers are defined in domain-specified versioned namespaces such that domain-specific tools do not have to process information from other domains.

## IP-XACT Enabled Implementations

As described in IEEE Std 1685TM-2009, Section 1.4.1, when modifying any existing IP-XACT descriptions, IP-XACT enabled design environments shall do so without losing any preexisting information. In particular, they shall preserve any vendor extension data included in the existing IP-XACT description.

In addition, IP-XACT enabled implementations that support Accellera vendor extensions shall not corrupt IP-XACT descriptions containing Accellera vendor extensions. More specifically, such implementations shall process name references implemented by the accellera:nameRef and accellera:viewNameRef elements correctly and avoid dangling name references.

## Outline

Section 2 defines the XML schema for the “accellera” namespace to describe the organization of Accellera extensions containers. Section 3 defines the XML schema for the “accellera-core” namespace to describe meta-data that is relevant in multiple domains. Section 4 defines the XML schema for the “accellera-ams” namespace to describe meta-data that is relevant in the analog and mixed signal domain. Section 5 defines the XML schema for the “accellera-pdp” namespace to describe meta-data that is relevant in physical design planning domain. Section 6 defines the XML schema for the “accellera-power” namespace to describe meta-data that is relevant in the powerl domain. Section7 describes the semantic consistency rules that need to be obeyed by vendor extensions in order to be valid Accellera vendor extensions.

# Accellera vendor extensions containers

## Containers

An *Accellera vendor extensions container* is a container for Accellera vendor extensions meta-data. All containers are defined in the namespace “accellera”. This namespace is not versioned to enable generic extensions support from IP-XACT enabled design environments and tools. The container name is identical to the spirit element name that it extends, except for the element names that exist in abstraction definitions which conflict with element names in components such as ports, port, wire, and transactional. The containers for these elements in abstraction definitions are prefixed with “logical” in order to distinguish them from the containers in components. In IEEE Std 1685TM-2009, some spirit elements have a vendor extension and some spirit elements do not have a vendor extension sub-element. For spirit elements that have a vendor extension sub-element, the container element must be located in that vendor extension sub-element. For spirit elements that do not have a vendor extension sub-element, the container element must be located in the nearest encapsulating spirit element that has a vendor extension sub-element.

### Schema

The following schema defines the Accellera vendor extensions container elements.



### Description

Each element of the **AccelleraVendorExtensionsExtensionsDocumentTypes** defines a container:

1. **accellera:logicalWire** (optional) specifies meta-data for wire ports in an abstraction definition.
2. **accellera:component** (optional) specifies meta-data for a component.
3. **accellera:view** (optional) specifies meta-data for a view in a component.
4. **accellera:port** (optional) specifies meta-data for a port in a component.
5. **accellera:wire** (optional) specifies meta-data for a wire port in a component.
6. **accellera:componentInstance** (optional) specifies meta-data for a component instance in a design.

### Example

This is an example of a component model wire port containing a standard extensions container. The declarations of the domain-specific namespaces are required only if they are actually used in the document.

<?xml version="1.0" encoding="UTF-8" standalone="yes"?>

<spirit:componentxsi:schemaLocation="  
http://www.spiritconsortium.org/XMLSchema/SPIRIT/1685-2009

http://www.accellera.org/XMLSchema/SPIRIT/1685-2009/index.xsd

http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE

http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE-1.0/index.xsd" xmlns:spirit="http://www.spiritconsortium.org/XMLSchema/SPIRIT/1685-2009" xmlns:accellera="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE" xmlns:accellera-core="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE/CORE-1.0" xmlns:accellera-ams="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE/AMS-1.0" xmlns:accellera-pdp="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE/PDP-1.0" xmlns:accellera-power="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE/POWER-1.0" xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance">

<spirit:vendor>accellera.org</spirit:vendor>

<spirit:library>ipxact</spirit:library>

<spirit:name>component</spirit:name>

<spirit:version>1.0</spirit:version>

<spirit:model>

<spirit:ports>

<spirit:port>

<spirit:name>myport</spirit:name>

<spirit:wire>

<spirit:direction>in</spirit:direction>

</spirit:wire>

<spirit:vendorExtensions>

<accellera:wire>

…

</accellera:wire>

</spirit:vendorExtensions>

</spirit:port>

</spirit:ports>

</spirit:model>

</spirit:component>

The next example shows a design component instance containing a standard extensions container.

<?xml version="1.0" encoding="UTF-8" standalone="yes"?>

<spirit:design xsi:schemaLocation="  
http://www.spiritconsortium.org/XMLSchema/SPIRIT/1685-2009

http://www.accellera.org/XMLSchema/SPIRIT/1685-2009/index.xsd

http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE

http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE-1.0/index.xsd" xmlns:spirit="http://www.spiritconsortium.org/XMLSchema/SPIRIT/1685-2009" xmlns:accellera="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE" xmlns:accellera-core="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE/CORE-1.0" xmlns:accellera-ams="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE/AMS-1.0" xmlns:accellera-pdp="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE/PDP-1.0" xmlns:accellera-power="http://www.accellera.org/XMLSchema/SPIRIT/1685-2009-VE/POWER-1.0" xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance">

<spirit:vendor>accellera.org</spirit:vendor>

<spirit:library>ipxact</spirit:library>

<spirit:name>design</spirit:name>

<spirit:version>1.0</spirit:version>

<spirit:componentInstances>

<spirit:componentInstance>

<spirit:instanceName>i\_component</spirit:instanceName>

<spirit:componentRef spirit:version="1.0" spirit:name="component"   
 spirit:library="ipxact" spirit:vendor="accellera.org"/>

<spirit:vendorExtensions>

<accellera:componentInstance>

…

</accellera:componentInstance>

</spirit:vendorExtensions>

</spirit:componentInstance>

</spirit:componentInstances>

</spirit:design>

## Name references

In containers it is possible to refer to **spirit:name** elements by using the **accellera:nameRef** element. Please see Section 5.2.3 for an example.

## View name references

In containers it is possible to refer to **spirit:name** elements inside view elements by using the **accellera:viewNameRef** element. Please see Section 3.2.3.3 for an example.

## Logical wire container

### Schema

The following schema defines the contents of the logical wire container.



### Description

The logical wire container contains Accellera vendor extensions in the power namespace.

## Component container

### Schema

The following schema defines the contents of the component container.



### Description

The component container contains Accellera vendor extensions in the power namespace.

## View container

### Schema

The following schema defines the contents of the view container.



### Description

The view container contains Accellera vendor extensions in the physical design planning namespace.

## Port container

### Schema

The following schema defines the contents of port container.



### Description

The port container contains Accellera vendor extensions in the core namespace.

## Wire container

### Schema

The following schema defines the contents of the wire container.



### Description

The wire container contains Accellera vendor extensions in the core, analog and mixed signal, physical design planning, and power namespaces.

## Component instance container

### Schema

The following schema defines the contents of the component instance container.



### Description

The component instance container contains Accellera vendor extensions in the power namespace.

# Core extensions

The core extensions are defined in the “accellera-core” namespace. The purpose of core extensions is to describe vendor extensions meta-data that is shared between domain-specific namespaces.

## Port extension

### Schema

The following schema defines the contents of the core port container.



### Description

The core port extension contains the following elements.

1. **accellera-core:portParameters** (optional) is a container for one or more port parameters; see Section 3.1.3.

### Port parameter

A port parameter differs from a spirit parameter element because it contains a vector element and it supports parameter value attributes unit and prefix.

#### Schema

The following schema defines the contents of the port parameter element.



#### Description

1. **spirit:nameGroup** group containing **name**, **displayName**, and **description**. The name together with the vector range shall be unique within the containing portParameters element.
2. **spirit:vector** (optional) determines on which port elements the parameter shall be applied.
3. **accellera-core:value** (mandatory) specifies the parameter value; see Section 3.3.

#### Example

This is an example of a port extension containing a port parameter.

<accellera:port>

<accellera-core:portParameters>

<accellera-core:portParameter>

<spirit:name>Voltage</spirit:name>

<accellera-core:value>1.3</accellera-core:value>

</accellera-core:portParameter>

</accellera-core:portParameters>

</accellera:port>

## Wire extension

### Schema

The following schema defines the contents of the core wire container.



### Description

The core wire extension contains the following elements.

1. **accellera-core:driver** (optional) defines a driver for the wire port; see Section 3.2.3.

### Driver

A driver differs from a spirit driver because it supports other values than non-negative integers.

#### Schema

The following schema defines the contents of the driver element.



#### Description

The driver element contains the following elements.

1. **accellera-core:defaultValue** (mandatory) representing a list of floats. Elements of a list match with the port elements from left to right in a vector.
2. **accellera:viewNameRef** (mandatory) ) indicates the view or views in which this driver applies. Multiple views can use the same set of type properties by specifying multiple **viewNameRef** elements. The **viewNameRef** shall match a **view name** in the containing object. The **viewNameRef** element is of type ***NMTOKEN***.

#### Example

This is an example of a driver extension.

<spirit:port>

<spirit:name>gnds</spirit:name>

<spirit:wire>

<spirit:direction>in</spirit:direction>

<spirit:driver>

<spirit:defaultValue>1</spirit:defaultValue>

</spirit:driver>

</spirit:wire>

<spirit:vendorExtensions>

<accellera:wire>

<accellera-core:driver>

<accellera-core:defaultValue>0.7</accellera-core:defaultValue>

<accellera:viewNameRef>functional-ams</accellera:viewNameRef>

</accellera-core:driver>

</accellera:wire>

</spirit:vendorExtensions>

</spirit:port>

## Value

A value differs from a spirit value because it supports two additional attributes prefix and unit.

### Schema

The following schema defines the contents of the value element.



### Description

The element **accellera-core:value** is configurable with attributes from spirit:string.prompt.att. In addition it has two optional attributes

1. **accellera-core:prefix** which can take the values in Table 1.
2. **accellera-core:unit** which can take the relevant units in Table 2 and Table 3, respectively, i.e., second, ampere, Kelvin, hertz, joule, watt, coulomb, volt, farad, ohm, Siemens, henry, Celsius.

Note that both **prefix** and **unit** can be used for documentation purposes only. The prefix attribute is not used to normalize the value to the base unit!

Table : Standard prefixes for the SI units [source: Wikipedia].



Table 2: SI base units [source: Wikipedia].



Table : Units derived from SI base units [source: Wikipedia].



### Example

This is an example of a port extension containing a port parameter with a value using the unit and prefix attributes.

<accellera:port>

<accellera-core:portParameters>

<accellera-core:portParameter>

<spirit:name>Voltage</spirit:name>

<accellera-core:value accellera-core:unit="volt" accellera-core:prefix="kilo">

1.3

</accellera-core:value>

</accellera-core:portParameter>

</accellera-core:portParameters>

</accellera:port>

# Analog and mixed signal extensions

The analog and mixed signal extensions are defined in the “accellera-ams” namespace. The purpose of analog and mixed signal extensions is to describe vendor extensions meta-data that enables integration of analog IPs as well as the mixture of analog and digital IPs.

## Wire extension

### Schema

The following schema defines the contents of the analog and mixed signal wire container.



### Description

The analog and mixed signal wire extension contains the following elements.

1. **accellera-ams:domainTypeDefs**  (optional) describes the domain type properties for a port per view of a component or abstractor. There can be an unbounded series of **accellera-ams:domainTypeDef**s defined for each port, allowing the type properties to be defined differently for each view; **domainTypeDef** is defined in Section 4.1.3.
2. **accellera-ams:signalTypeDefs** (optional) describes the signal type properties for a port per view of a component or abstractor. There can be an unbounded series of **accellera-ams:signalTypeDef**s defined for each port, allowing the type properties to be defined differently for each view; **signalTypeDef** is defined in Section 4.1.4.

### Domain type definition

#### Schema

The following schema defines the contents of a domain type definition.



#### Description

A domain type definition contains the following elements.

1. **accellera-ams:typeName** (mandatory) defines the name of the domain type for the port. For VHDL, some typical values would be ddiscrete and electrical. The domainTypeNameelement is of type ***string***.
2. **accellera-ams:typeDefinition** (optional) contains a language-specific reference to where the given type is actually defined. There can be multiple **typeDefinition**s for each port. The **typeDefinition** element is of type ***string***.
3. **accellera:viewNameRef** (mandatory) indicates the view or views in which this type definition applies. Multiple views can use the same set of type properties by specifying multiple **viewNameRef** elements. The **viewNameRef** shall match a **view name** in the containing object. The **viewNameRef** element is of type ***NMTOKEN***.

### Signal type definition

#### Schema

The following schema defines the contents of a domain type definition.



#### Description

A signal type definition contains the following elements.

1. **accellera-ams:signalType** (mandatory) defines the signal type for the port. **Continuous-conservative** is a signal which is continuous in time and quantity, where the quantity represents voltage and current to capture the conservative behavior of an electrical network (i. e. Kirchhoff’s Laws apply), and which has no direction. **Continuous-non-conservative** is a directed signal which is continuous in time and quantity, where the quantity represents either a voltage or a current (often called signal flow). In this case it only captures the non-conservative behavior of a set of interconnected components. **Discrete** is a directed sampled signal which is time-discrete and value-continuous (the value may also be quantified), where the value represents either a voltage or a current (other representations are possible also). It captures the non-conservative behavior of a set of interconnected components.
2. **accellera:viewNameRef** (mandatory) indicates the view or views in which this type definition applies. Multiple views can use the same set of type properties by specifying multiple **viewNameRef** elements. The **viewNameRef** shall match a **view name** in the containing object. The **viewNameRef** element is of type ***NMTOKEN***.

Table 4 shows the mapping of the three signal types onto VHDL, Verilog, and SystemC AMS types.

Table : Mapping of signal types onto data types in various HDLs.

|  |  |  |  |
| --- | --- | --- | --- |
| **signalType** | **VHDL-AMS** | **Verilog-AMS** | **SystemC-AMS** |
| continuous conservative | terminal outp : electrical; | electrical outp; | sca\_eln::sca\_terminal outp;1) |
| continuous  non-conservative | quantity outp : out real; | sf\_voltage outp; 2) | sca\_lsf::sca\_out outp; 1) |
| discrete | signal outp : out real; | wreal outp;  ddiscrete outp; 3) | sca\_tdf::sca\_out<double> outp; |

Notes:

1. SystemC-AMS 1.0 only supports linear electrical networks (ELN) and linear signal flow (LSF).
2. voltage is defined as: discipline sf\_voltage; potential Voltage; enddiscipline. The discipline sf\_voltage declaration must be described in a **domainTypeDef**.
3. ddiscrete is defined as: discipline ddiscrete; domain discrete; enddiscipline The discipline ddiscrete declaration must be described in a **domainTypeDef**.

### Example

This is an example of domainTypeDefs and signalTypeDefs.

<spirit:port>

<spirit:name>myport</spirit:name>

<spirit:wire>

<spirit:direction>in</spirit:direction>

</spirit:wire>

<spirit:vendorExtensions>

<accellera:wire>

<accellera-ams:domainTypeDefs>

<accellera-ams:domainTypeDef>

<accellera-ams:domainTypeName>electrical</accellera-ams:domainTypeName>

<accellera-ams:typeDefinition>disciplines.vams

</accellera-ams:typeDefinition>

<accellera:viewNameRef>functional-ana</accellera:viewNameRef>

</accellera-ams:domainTypeDef>

</accellera-ams:domainTypeDefs>

<accellera-ams:signalTypeDefs>

<accellera-ams:signalTypeDef>

<accellera-ams:signalType>continuous-conservative</accellera-ams:signalType>

<accellera:viewNameRef>functional-ana</accellera:viewNameRef>

</accellera-ams:signalTypeDef>

<accellera-ams:signalTypeDef>

<accellera-ams:signalType>discrete</accellera-ams:signalType>

<accellera:viewNameRef>functional-sca-tdf</accellera:viewNameRef>  
 </accellera-ams:signalTypeDef>

</accellera-ams:signalTypeDefs>

</accellera:wire>

</spirit:vendorExtensions>

</spirit:port>

# Physical design planning extensions

The physical design planning extensions are defined in the “accellera-pdp” namespace. The purpose of physical design planning extensions is to describe vendor extensions meta-data that enables automation of ASIC and FPGA implementation flows.

## View extension

### Schema

The following schema defines the contents of the physical design planning view container.



### Description

The physical design planning view extension contains the following elements.

1. **accellera-pdp:technologyName** (optional) describing the name of the technology. This element has a mandatory attribute **accellera-pdp:type** that can take the values ASIC and FPGA indicating the type of technology.
2. **accellera-pdp:areaEstimation (**optional) describing properties of the view in the specified technology. The elements of **areaEstimation** are described in Section 5.1.3

### Area estimation

#### Schema

The following schema defines the contents of the area estimation element.



#### Description

The area estimation contains the following elements.

1. **accellera-pdp:gateArea** describing the standard cell area (in mm2 or number of logic cells depending on the technology type ASIC or FPGA, respectively) out of synthesis without taking into account any extra space.
2. **accellera-pdp:macroArea** (optional) describing area (in mm2 or number of logic cells depending on the technology type ASIC or FPGA, respectively) of the other cells (macro, memories) that are part of the component. If not present, then the value is assumed to be zero, i.e., the component is assumed to be made of logic cells only.
3. **accellera-pdp:maxMacroWidth** (optional) describing the width in mm of the biggest macro that may constrain the component floor plan.
4. **accellera-pdp:maxMacroHeight** (optional) describing the height in mm of the biggest macro that may constrain the component floor plan.
5. **accellera-pdp:totalArea** (optional) describing the estimated area (in mm2 or number of logic cells depending on the technology type ASIC or FPGA, respectively) of the component after physical implementation. The difference between **totalArea** and the sum of **gateArea** and **macroArea** typically represents provision for routing, congestion and floor plan constraints as estimated by the provider.

The values may be dependent on one or more parameters to account for configurable IPs.

### Example

This is an example of a physical design planning view extension.

<spirit:view>

<spirit:name>layout</spirit:name>

<spirit:envIdentifier>:\*Layout:</spirit:envIdentifier>

<spirit:vendorExtensions>

<accellera:view>

<accellera-pdp:technologyName type="asic">cmos032lp  
 </accellera-pdp:technologyName>

<accellera-pdp:areaEstimation>

<accellera-pdp:maxMacroWidth spirit:resolve="immediate">0.02  
 </accellera-pdp:maxMacroWidth>

<accellera-pdp:gateArea spirit:resolve="dependent"  
 spirit:dependency="id(‘param1’)\*1.24">1.24

</accellera-pdp:gateArea>

<accellera-pdp:macroArea spirit:resolve="dependent"  
 spirit:dependency="id(‘param1’)\*0.2">0.2  
 </accellera-pdp:macroArea>

<accellera-pdp:maxMacroHeight spirit:resolve="dependent"   
 spirit:dependency="id(‘param1’)\*0.01">0.01  
 </accellera-pdp:maxMacroHeight>

<accellera-pdp:totalArea spirit:resolve="dependent"  
 spirit:dependency="id(‘param1’)\*1.44">1.50  
 </accellera-pdp:totalArea>

</accellera-pdp:areaEstimation>

</accellera:view>

</spirit:vendorExtensions>

</spirit:view>

## Wire extension

### Schema

The following schema defines the contents of the physical design planning wire container.



### Description

The physical design planning wire container has the following elements.

1. **accellera-pdp:registerCount** (optional) specifies the number of sequential elements (i.e. leaf cells) seen by this port in case it is a clock source. This value may be dependent on one or more parameters to account for configurable IPs.
2. **accellera-pdp:combinationalPaths** (optional) is a list of combinational paths crossing the component by means of this output port (sink) directly dependent on input ports (sources); it is defined in Section 5.2.3.

### Combinational paths

#### Schema

The following schema defines the contents of the combinational path element.



#### Description

The combinational path element contains the following elements.

1. **spirit:vector** (optional) describing the range of the port to which the combinational path applies
2. **accellera-pdp:sources** (mandatory) is a list of **accellera-pdp:source** elements. Each source element has a mandatory **accellera:nameRef** element referring to an input port and an optional **spirit:vector** element indicating the range of that input port.

### Example

This is an example of a physical design planning wire extension.

<spirit:port>

<spirit:name>myoutput</spirit:name>

<spirit:wire>

<spirit:direction>out</spirit:direction>

</spirit:wire>

<spirit:vendorExtensions>

<accellera:wire>

<accellera-pdp:combinationalPaths>

<accellera-pdp:combinationalPath>

<spirit:vector>

<spirit:left>0</spirit:left>

<spirit:right>0</spirit:right>

</spirit:vector>

<accellera-pdp:sources>

<accellera-pdp:source>

<spirit:name>myinput1</spirit:name>

<spirit:vector>

<spirit:left>5</spirit:left>

<spirit:right>5</spirit:right>

</spirit:vector>

</accellera-pdp:source>

<accellera-pdp:source>

<spirit:name>myinput2</spirit:name>

</accellera-pdp:source>

</accellera-pdp:sources>

</accellera-pdp:combinationalPath>

</accellera-pdp:combinationalPaths>

</accellera:wire>

</spirit:vendorExtensions>  
</spirit:port>

# Power extensions

The power extensions are defined in the “accellera-power” namespace. The purpose of power extensions is to describe vendor extensions meta-data that enables automation of power flows.

## Logical wire extension

### Schema

The following schema defines the content of the power logical wire container.****

### Description

The logical wire power container contains the following elements.

1. **accellera-power:domain** (optional) specifies the power domain. It is the user’s responsibility to ensure it matches with an existing power domain in an UPF/CPF file.
2. **accellera-power:isolation** (optional) specifies the isolation value. Common values are 0, 1, L (latched), Z (high impedance), N (no isolation needed - default value), and X (isolation needed - no value specified).
3. **accellera-power:idle** (optional) is a string value. The output value for each bit of the port in idle mode. Only applies for output ports.
4. **accellera-power:reset** (optional) is a String value. The output value for each bit of the port in reset mode. Only applies for output ports.
5. **spirit:vector** (optional) is a vector specifying for which port elements this power description applies.

### Example

This is an example of a logical wire power extension.

<spirit:abstractionDefinition …>

<spirit:vendor>accellera.org</spirit:vendor>

<spirit:library>library</spirit:library>

<spirit:name>absdef</spirit:name>

<spirit:version>1.0</spirit:version>

<spirit:busType spirit:vendor="accellera.org" spirit:library="library"  
 spirit:name="busdef" spirit:version="1.0"/>

<spirit:ports>

<spirit:port>

<spirit:logicalName>lo1</spirit:logicalName>

<spirit:wire/>

</spirit:port>

<spirit:port>

<spirit:logicalName>lo2</spirit:logicalName>

<spirit:wire/>

<spirit:vendorExtensions>

<accellera:logicalWire>

<accellera-power:logicalWirePowerDefs>

<accellera-power:logicalWirePowerDef>

<accellera-power:domain>domain4</accellera-power:domain>

<accellera-power:isolation>Z</accellera-power:isolation>

<accellera-power:idle>1</accellera-power:idle>

<accellera-power:reset>0</accellera-power:reset>

</accellera-power:logicalWirePowerDef>

</accellera-power:logicalWirePowerDefs>

</accellera:logicalWire>

</spirit:vendorExtensions>

</spirit:port>

</spirit:ports>

</spirit:abstractionDefinition>

## Component extension

### Schema

The following schema defines the content of the power component container.



### Description

The power component container contains the following elements.

1. **accellera-power:domain** (optional) specifies the power domain. It is the user’s responsibility to ensure it matches with an existing power domain in an UPF/CPF file.
2. **accellera-power:isolation** (optional) specifies the isolation value. Common values are 0, 1, L (latched), Z (high impedance), N (no isolation needed - default value), and X (isolation needed - no value specified).
3. **accellera-power:retentionMode** (optional) is a boolean value. If set to true, then the component needs retention for all internal registers.
4. **accellera-power:alwaysPowered** (optional) is a boolean value. If set to true, then the component is always powered, whatever its power domain. Only applies for output ports.
5. **accellera-power:idle** (optional) is a string value. The output value for each bit of the component in idle mode. Only applies for output ports.
6. **accellera-power:reset** (optional) is a String value. The output value for each bit of the component in reset mode. Only applies for output ports.
7. **accellera-power:hasIsolation** (optional) is a boolean value. If set to true, then the component already has an isolation feature embedded.
8. **accellera-power:hasLevelShifter** (optional) is a boolean value. If set to true, then the component already has a level shifter embedded.

### Example

This is an example of a component power extension.

<spirit:component …>

<spirit:vendor>accellera.org</spirit:vendor>

<spirit:library>library</spirit:library>

<spirit:name>component</spirit:name>

<spirit:version>1.0</spirit:version>

<spirit:vendorExtensions>

<accellera:component>

<accellera-power:componentPowerDef>

<accellera-power:domain>mydomain</accellera-power:domain>

<accellera-power:isolation>0</accellera-power:isolation>

</accellera-power:componentPowerDef>

</accellera:component>

</spirit:vendorExtensions>

</spirit:component>

## Wire extension

### Schema

The following schema defines the content of the power wire container.



### Description

The power wire container contains the following elements.

1. **accellera-power:domain** (optional) specifies the power domain. It is the user’s responsibility to ensure it matches with an existing power domain in an UPF/CPF file.
2. **accellera-power:isolation** (optional) specifies the isolation value. Common values are 0, 1, L (latched), Z (high impedance), N (no isolation needed - default value), and X (isolation needed - no value specified).
3. **accellera-power:idle** (optional) is a string value. The output value for each bit of the port in idle mode. Only applies for output ports.
4. **accellera-power:reset** (optional) is a String value. The output value for each bit of the port in reset mode. Only applies for output ports.
5. **accellera-power:hasIsolation** (optional) is a boolean value. If set to true, then the port already has an isolation feature embedded.
6. **accellera-power:hasLevelShifter** (optional) is a boolean value. If set to true, then the port already has a level shifter embedded.
7. **spirit:vector** (optional) is a vector specifying for which port elements this power description applies.

### Example

This is an example of a wire power extension.

<spirit:port>

<spirit:name>pc</spirit:name>

<spirit:wire>

<spirit:direction>in</spirit:direction>

<spirit:vector>

<spirit:left>7</spirit:left>

<spirit:right>0</spirit:right>

</spirit:vector>

</spirit:wire>

<spirit:vendorExtensions>

<accellera:wire>

<accellera-power:wirePowerDefs>

<accellera-power:wirePowerDef>

<accellera-power:domain>domain2</accellera-power:domain>

<accellera-power:isolation>L</accellera-power:isolation>

</accellera-power:wirePowerDef>

<accellera-power:wirePowerDef>

<accellera-power:domain>domain3</accellera-power:domain>

<spirit:vector>

<spirit:left>3</spirit:left>

<spirit:right>0</spirit:right>

</spirit:vector>

</accellera-power:wirePowerDef>

</accellera-power:wirePowerDefs>

</accellera:wire>

</spirit:vendorExtensions>

</spirit:port>

## Component instance extension

### Schema

The following schema defines the content of the power component instance container.



### Description

The power component instance container contains the following elements.

1. **accellera-power:componentInstancePowerDef** (optional) specifies the power information for component instances. This element is a component power definition as defined in Section 6.2.
2. **accellera-power:wireInstancePowerDefs** (optional) the power information for component instances. This element is a wire power definition as defined in Section 6.4.3.1.

### Example

This is an example of a component instance power extension.

<spirit:componentInstance>

<spirit:instanceName>myip1</spirit:instanceName>

<spirit:componentRef spirit:vendor="Mds" spirit:library="test" spirit:name="comp"

spirit:version="1.0"/>

<spirit:vendorExtensions>

<accellera:componentInstance>

<accellera-power:componentInstancePowerDef>

<accellera-power:domain>domain6</accellera-power:domain>

<accellera-power:isolation>L</accellera-power:isolation>

<accellera-power:idle>1</accellera-power:idle>

<accellera-power:reset>1</accellera-power:reset>

</accellera-power:componentInstancePowerDef>

</accellera:componentInstance>

</spirit:vendorExtensions>

</spirit:componentInstance>

#### Wire instance power definition

The following schema defines the content of the wire instance power definition.



#### Description

The power wire instance port power definition contains an **accellera:nameRef** element specifying the name of component port for which this wire instance port power definition applies. All other elements are identical to the elements in a wire port power definition described in Section 6.3.

#### Example

This is an example of a wire instance power extension within a component instance power extension.

<spirit:componentInstance>

<spirit:instanceName>myip1</spirit:instanceName>

<spirit:componentRef spirit:vendor="Mds" spirit:library="test" spirit:name="comp"

spirit:version="1.0"/>

<spirit:vendorExtensions>

<accellera:componentInstance>

<accellera-power:wireInstancePowerDefs>

<accellera-power:wireInstancePowerDef>

<accellera:nameRef>pd</accellera:nameRef>

<accellera-power:domain>domain7</accellera-power:domain>

<accellera-power:isolation>X</accellera-power:isolation>

</accellera-power:wireInstancePowerDef>

</accellera-power:wireInstancePowerDefs>

</accellera:componentInstance>

</spirit:vendorExtensions>

</spirit:componentInstance>

# Semantic Consistency Rules

Accellera vendor extensions need to obey to the following semantic consistency rules in order to be valid.

## Core Rules

Table : Core semantic consistency rules.

|  |  |  |  |
| --- | --- | --- | --- |
| Rule Number | Rule | Single doc check | Notes |
| SCR CORE.1 | The vector of a portParameter must be a sub-vector of the port. | yes | See also 3.1.3. |
| SCR CORE.2 | The vectors of two portParameters of the same port that have the same portParameter names cannot overlap. | yes | See also 3.1.3. |
| SCR CORE.3 | A port with direction out shall not have a driver extension | yes | See also 3.2.3. |
| SCR CORE.4 | The number of values in a defaultValue must be equal to the number of port elements. | yes | See also 3.2.3. |

## Analog and Mixed Signal Rules

Table : Analog and mixed signal semantic consistency rules.

|  |  |  |  |
| --- | --- | --- | --- |
| Rule Number | Rule | Single doc check | Notes |
| SCR AMS.1 | A component port with direction out and an analog and mixed signal extension does not count in a port connection equivalence class, i.e., multiple drivers are allowed on analog and mixed signals. | no | See also SCR 6.9. |

## Physical Design Planning Rules

Table : Physical design planning semantic consistency rules.

|  |  |  |  |
| --- | --- | --- | --- |
| Rule Number | Rule | Single doc check | Notes |
| SCR PDP.1 | totalArea should be at least equal to the sum of gateArea and macoArea | yes | See also 5.1.3. |
| SCR PDP.2 | A view containing areaEstimation must have a technologyName with a type attribute value . | yes | See also 5.1. |
| SCR PDP.3 | A view containing areaEstimation must have an envIdentifier containing “Layout” | yes | See also 5.1. |
| SCR PDP.4 | if a view refers to a file set with a LEF or XDC files, then it cannot contain an areaEstimation. | yes | See also 5.1. |
| SCR PDP.5 | Only input ports can have registerCounts. | yes | See also 5.2. |
| SCR PDP.6 | A port with a registerCount must be mapped in an interface onto a logical port with the isClock qualifier. | yes | See also 5.2. |
| SCR PDP.7 | In a combinationalPath, both sink and source must be a single bit. | yes | See also 5.2. |
| SCR PDP.8 | Files in file sets referenced from a view containing a technologyName with a type equal to “ASIC” or “FPGA” must be of userFileType “LEF” or “XDC”, respectively. | yes | See also 5.1. |

## Power Rules

Table : Power semantic consistency rules.

|  |  |  |  |
| --- | --- | --- | --- |
| Rule Number | Rule | Single doc check | Notes |
| SCR PWR.1 | The vector of a logical or component port power extension must be a sub-vector of the port. | yes | See also 6.1and 6.3. |
| SCR PWR.2 | The vectors of two logical or component port power extensions of the same port cannot overlap. | yes | See also 6.1and 6.3. |
| SCR PWR.3 | Only a logical or component port with direction out can contain an idle element. | yes | See also 6.1and 6.3. |
| SCR PWR.4 | Only a logical or component port with direction out can contain a reset element. | yes | See also 6.1and 6.3. |
| SCR PWR.5 | Power extensions have priorities. Component instance extensions have priority over component port extensions. Component port extensions have priority over component extensions. Component extensions have priority over logical port extensions. | no | See also 6.1, 6.2, 6.3, and 6.4. |
| SCR PWR.6 | The value of a domain element in a power extension must match with a power domain in a UPF/CPF file. | Requires external knowledge | See also 6.1, 6.2, 6.3, and 6.4. |