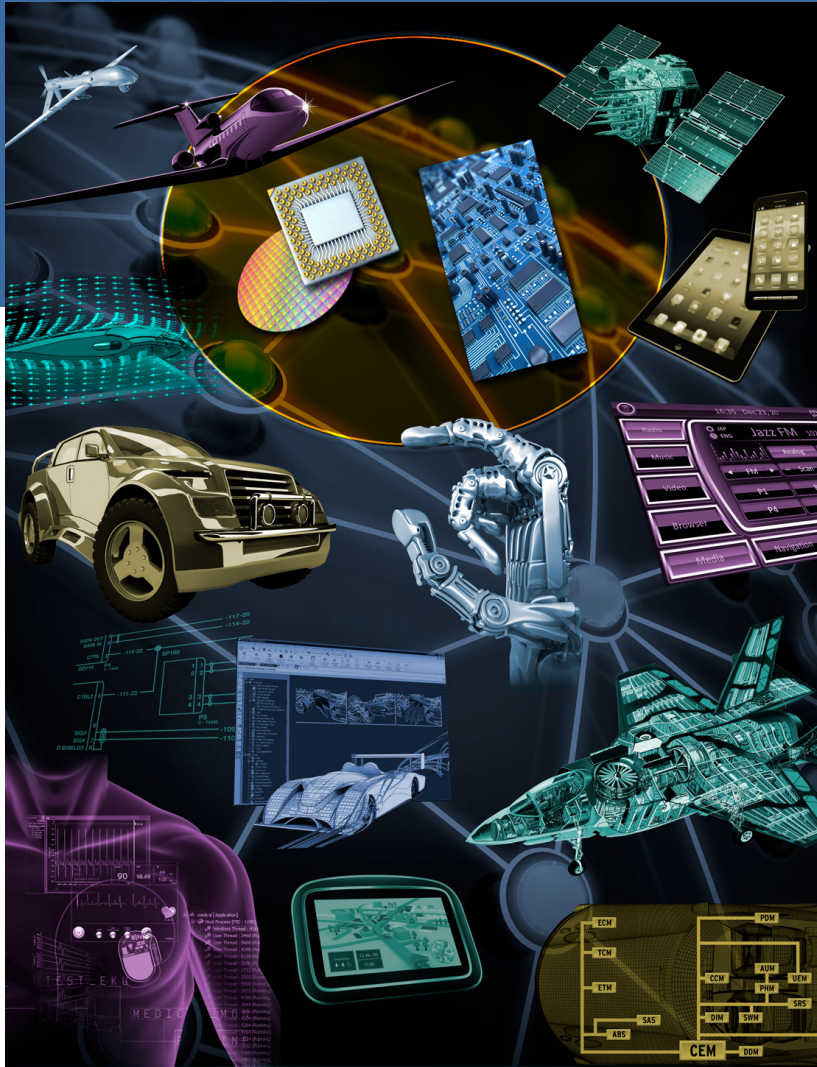


Verify Tomorrow's Systems: The Impact on Standards and Methodologies

Dennis Brophy

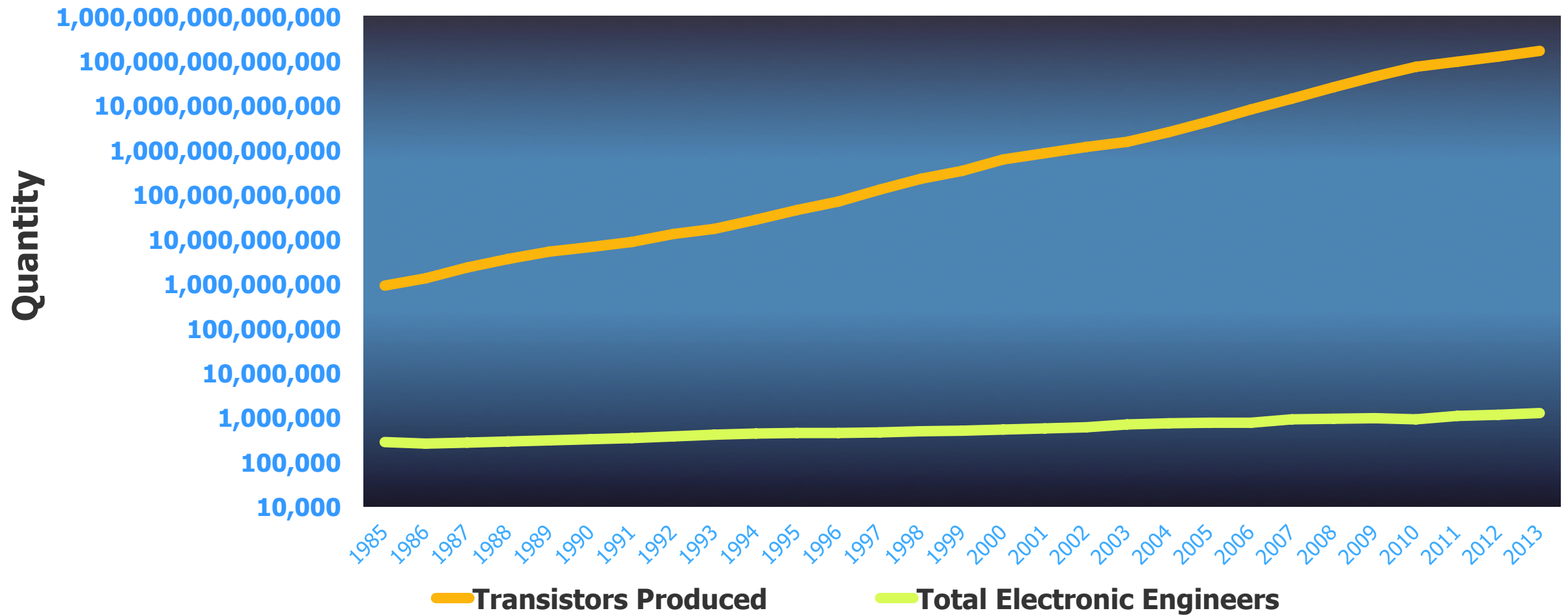
Director of Strategic Business Development
IC Verification Solutions Division

April 21, 2017



DESIGN PRODUCTIVITY

Design Productivity Grew 5 Orders of Magnitude Since 1985

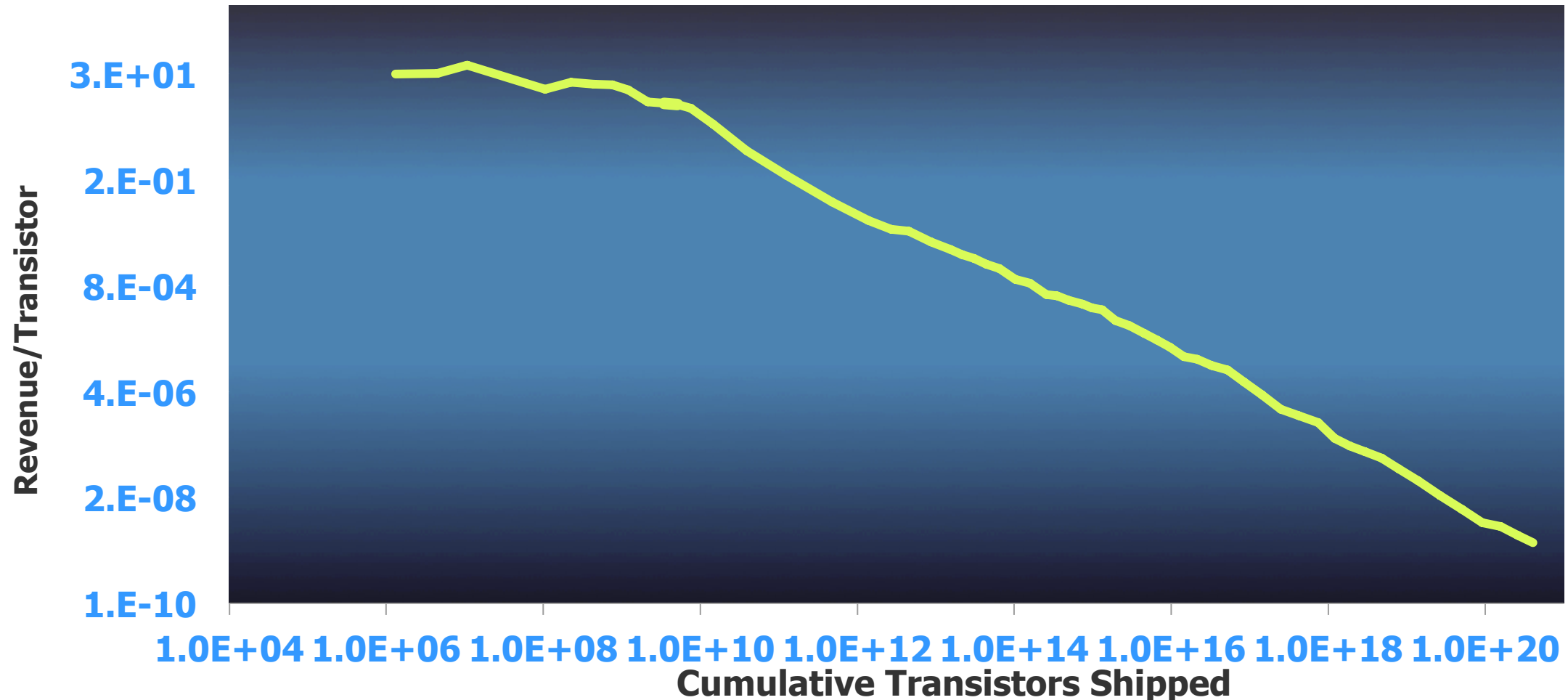


Source: Technology Research Group – EDA Database, 1986, EDA TAM, 1989 & Gartner/Dataquest 2005 Seat Count Report, Gary Smith EDA, 2013 Seat Count Analysis, VLSI Research, 2013 - Transistors Produced Analysis

Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

Cost Learning Curve Continues With or Without Moore's Law



Semiconductor Learning Curve 1954-2012 Adjusted for Inflation

Source: VLSI Research, SIA, Federal Reserve

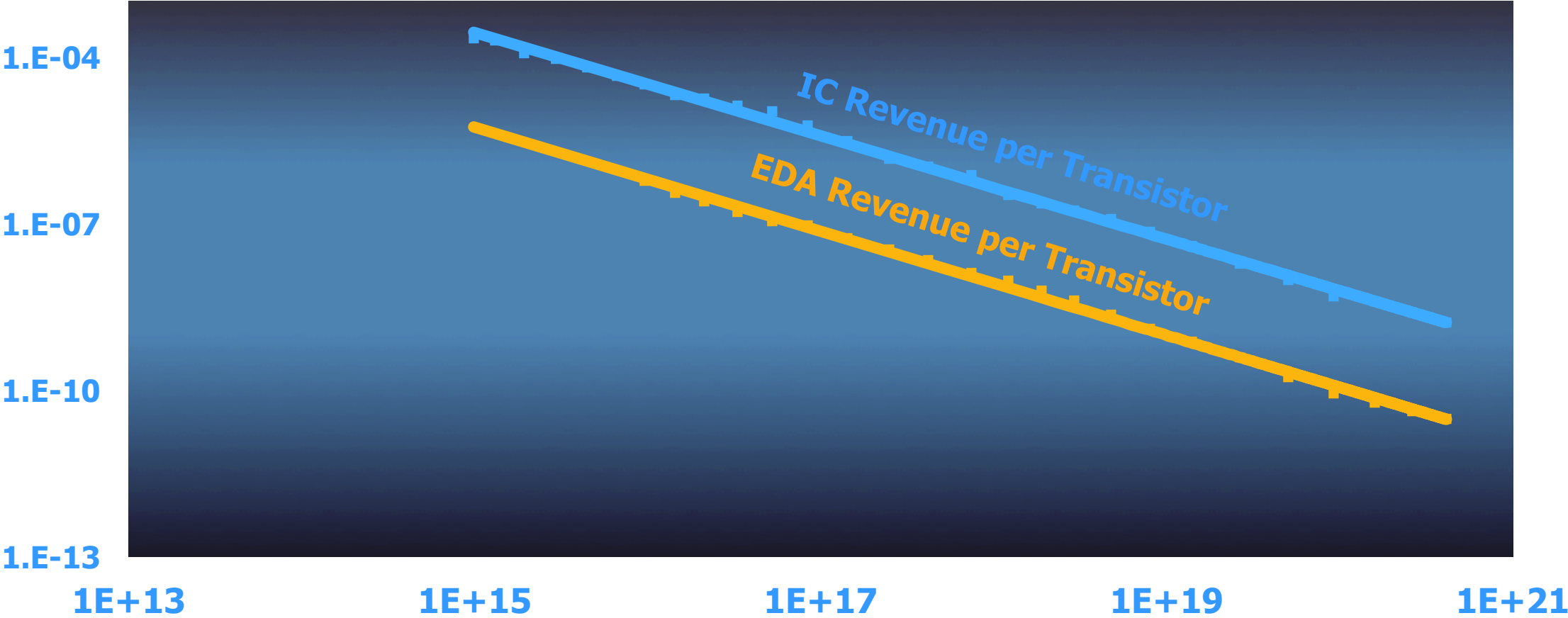
Note: Revenue adjusted for Inflation... 1954-2012

Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

Cost of EDA Software Decreases at the Same Rate as the Revenue per Transistor

Learning Curve
Revenue (\$)/Transistor

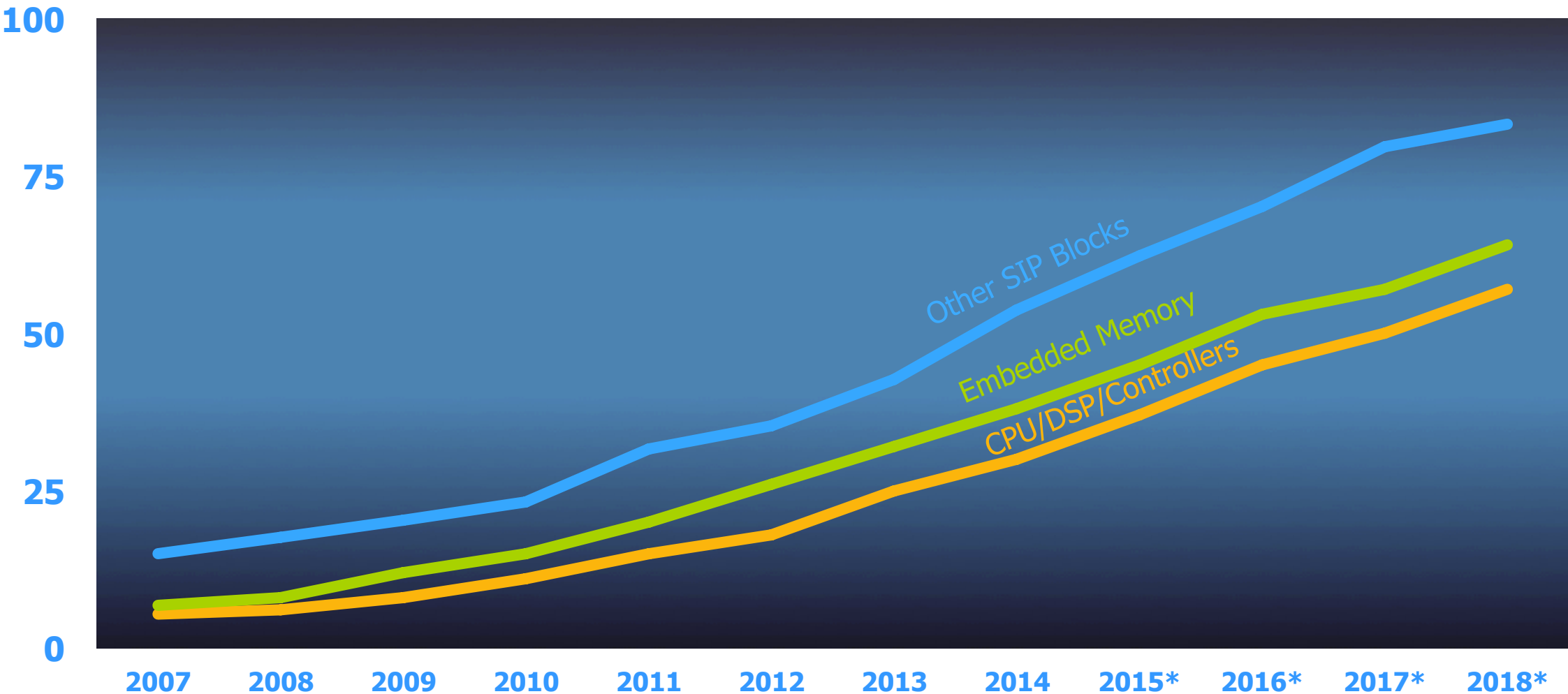


Note: EDA Cost Consists of EDA License and Maintenance revenue adjusted for Inflation

Source: VLSI Research, EDAC Market Statistics Service, Federal Reserve

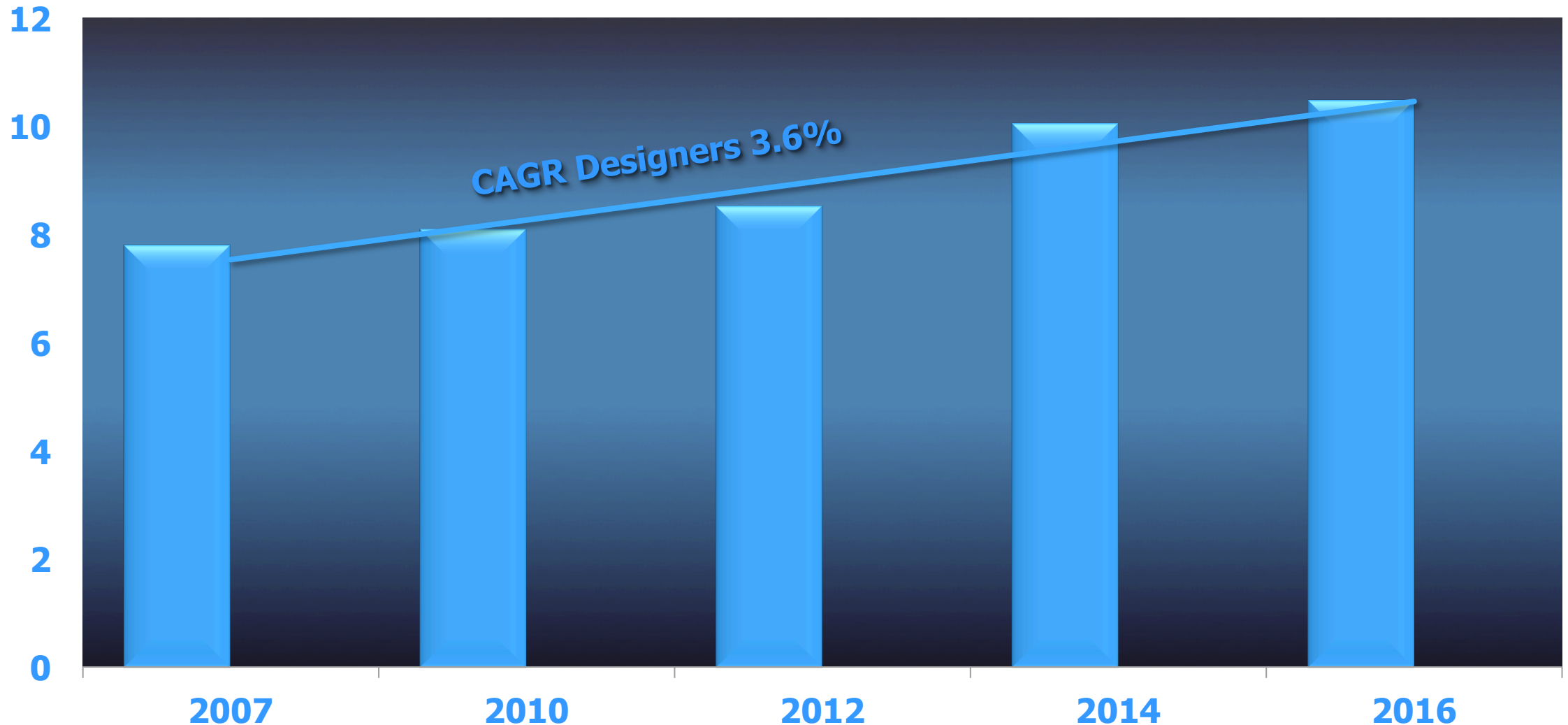
Restricted © 2017 Mentor Graphics Corporation

IP Reuse Has Driven a Large Share of Recent Design Productivity Gains



Source: Semico Research Corp. *Forecast

Demand for Design Engineers Grows Slowly

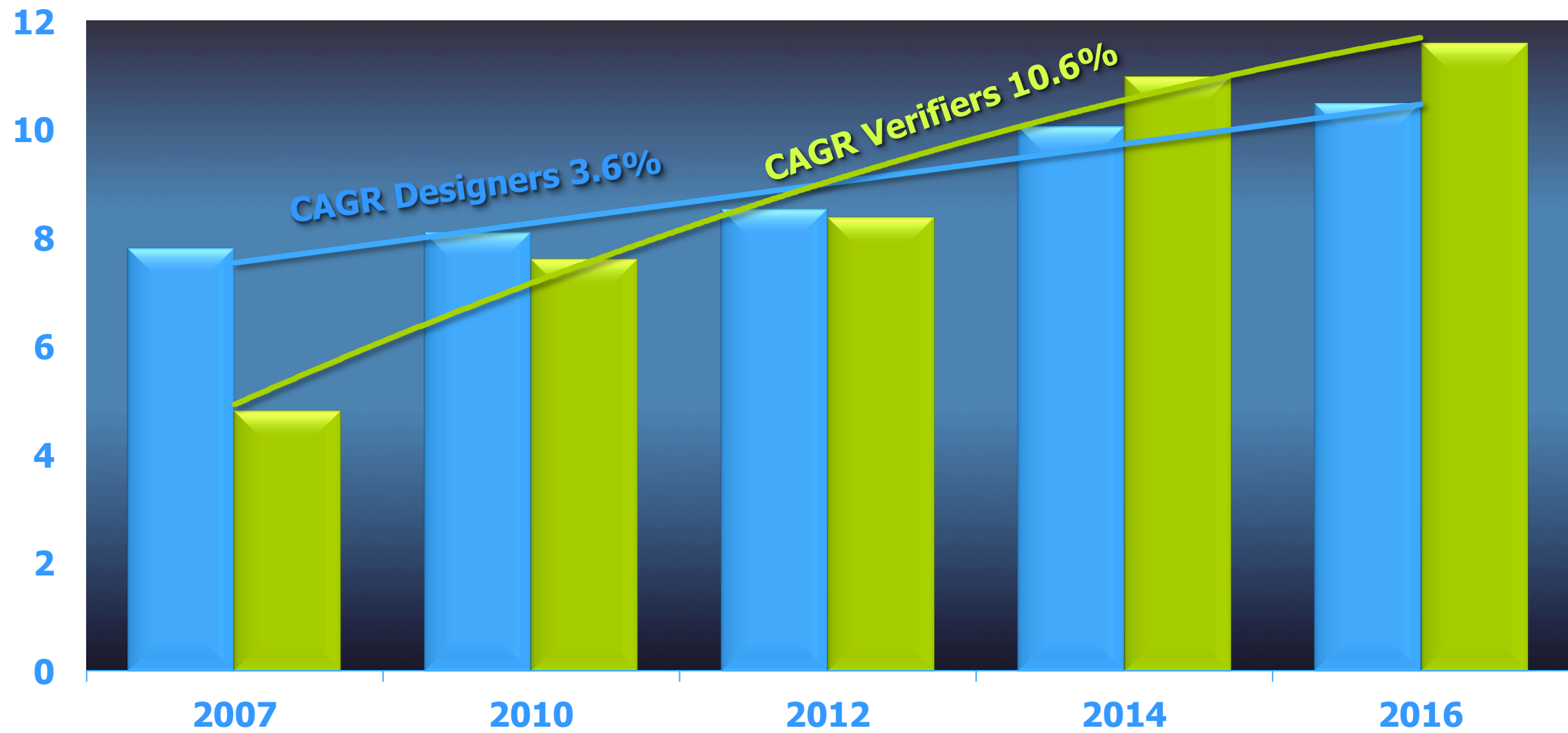


Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

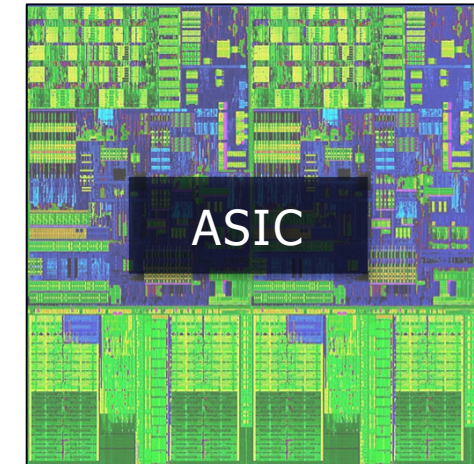
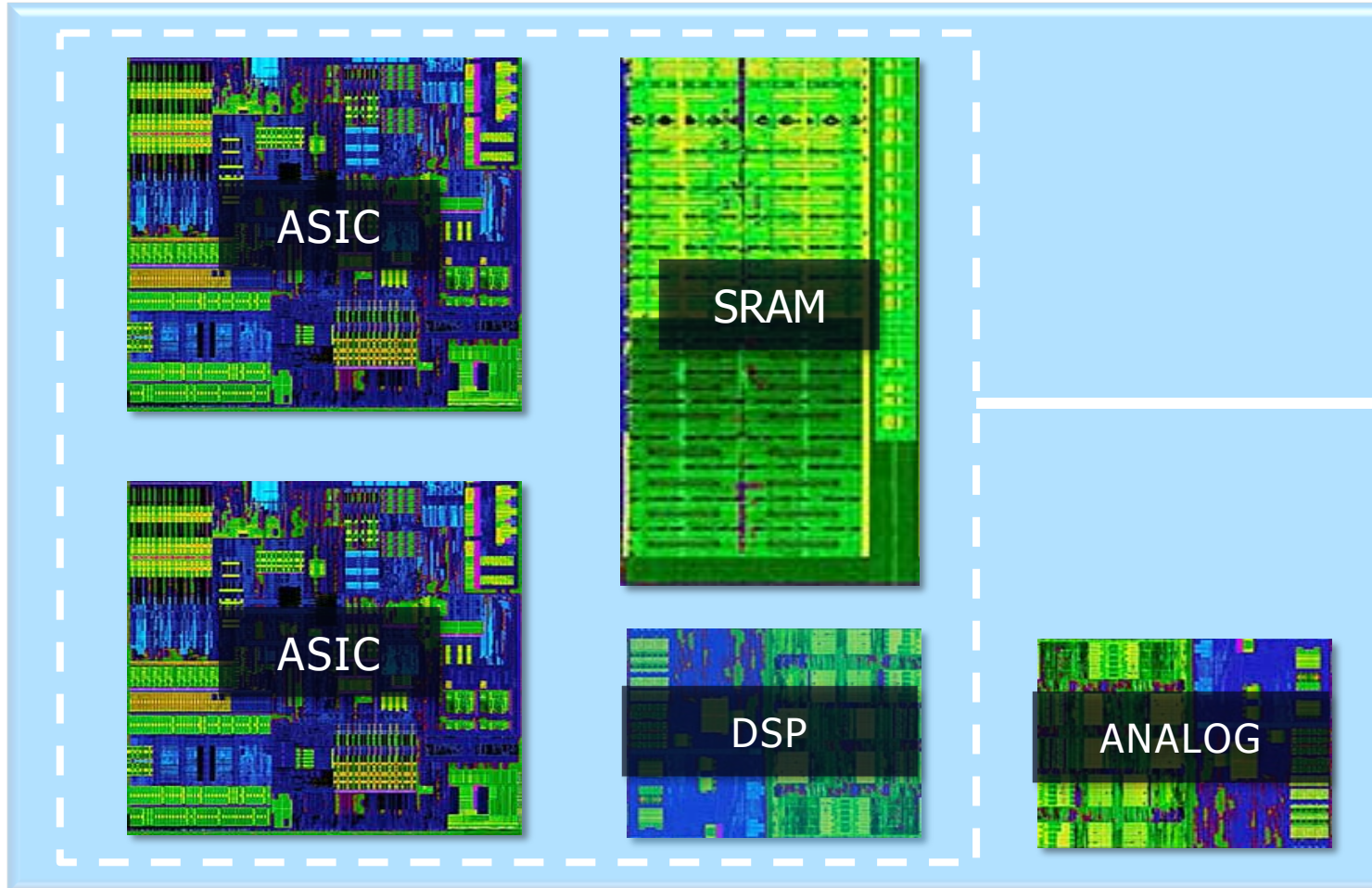
Verification Engineers Increase at 3X the Rate of Increase of Designers



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Restricted © 2017 Mentor Graphics Corporation

Upper Bound of Verification Cycle Requirements Increases 2^x



$$x = \text{memory bits} + \text{flip-flops} + \text{latches} + \text{I/O}$$

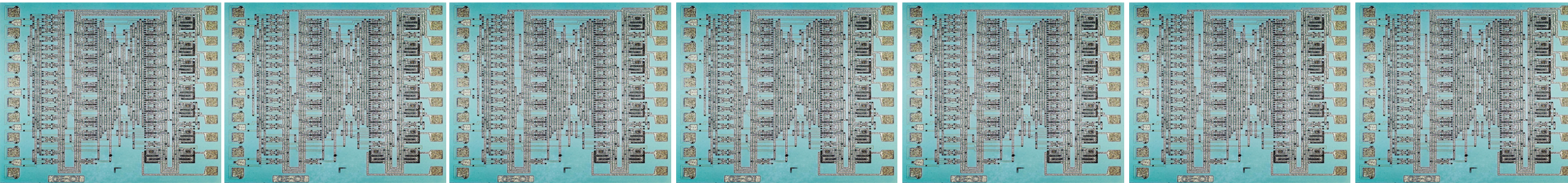
HOW DID WE GET HERE? A LOOK BACK...



Large Scale Integration (LSI) Evolves to VLSI

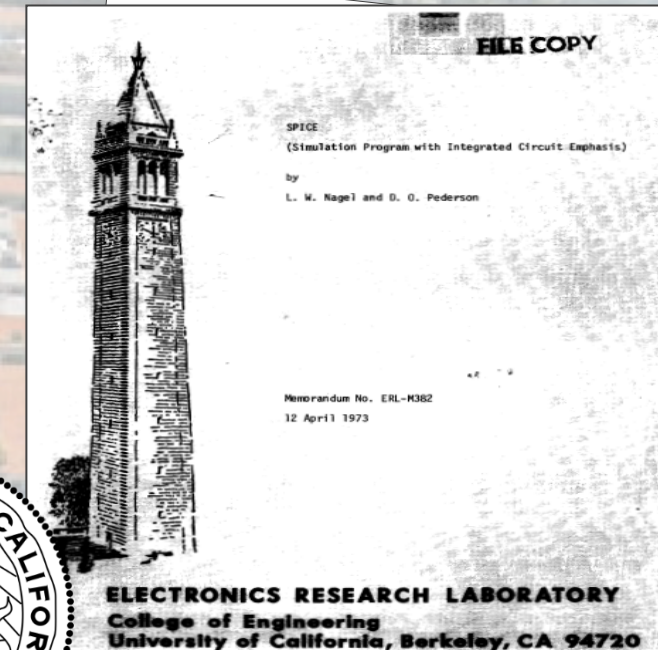


- SSI/MSI design and verify
 - Manual design and layout
 - Fabricate it
 - Test it
 - Re-design it
 - Repeat



Transistor-Level Simulation

- **CANCER**
 - Ron Roher
- **SPICE** – Simulation Program with Integrated Circuit Emphasis
 - L.W. Nagel and D.O. Pederson
 - Presented April 12, 1973



Larger Designs Required Gate-Level Simulation

VERIFICATION 0.0



Mentor Graphics – 1982 IDEA Station – QuickSim

QuickSim

Performance:

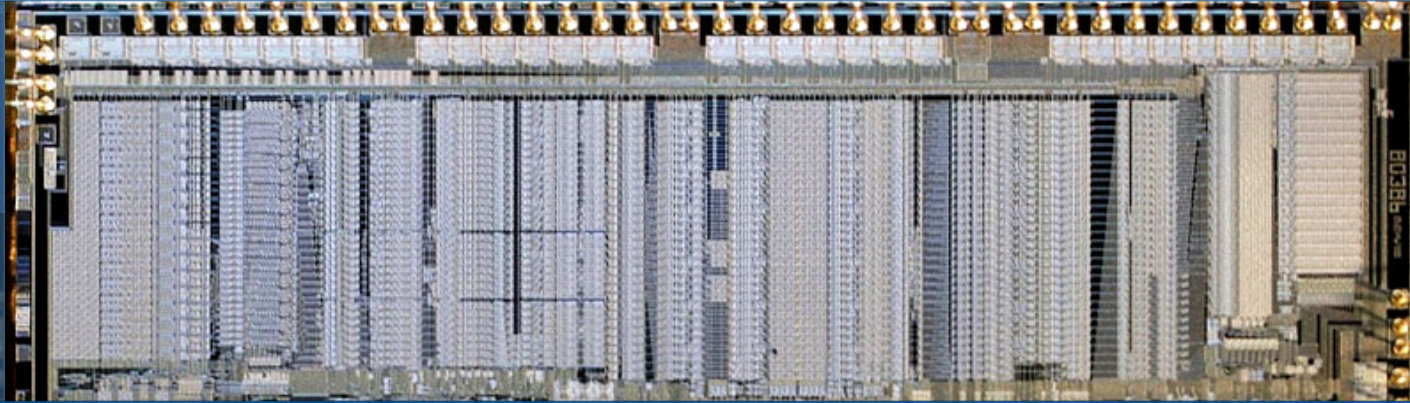
Workstation dependent

Capacity:

Workstation dependent

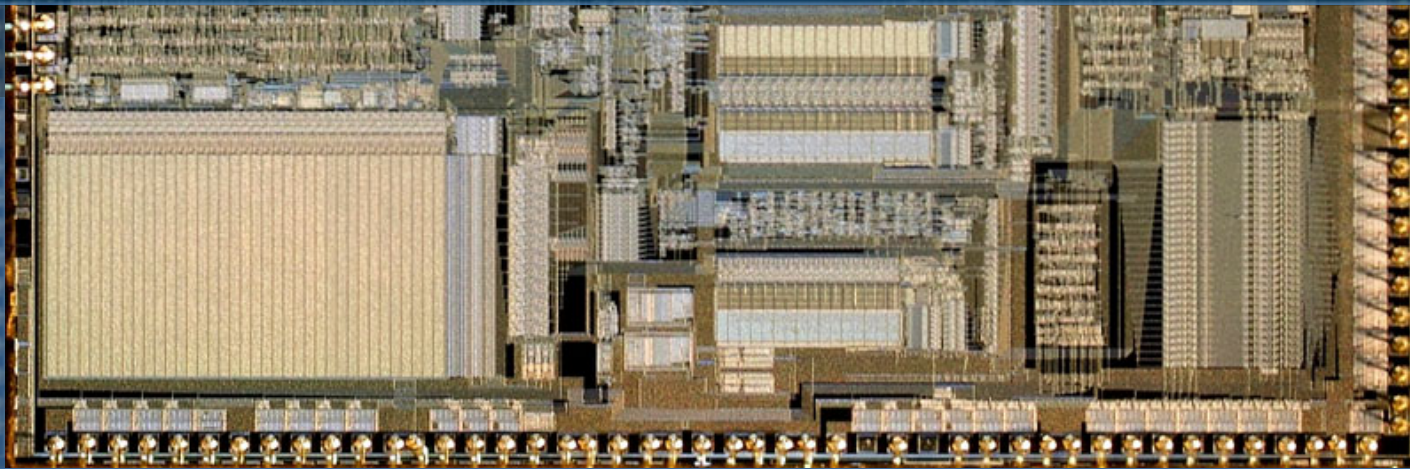
100K+ gates when gate-level models are used, much larger when functional or behavioral modeling methods are used

VERIFICATION 1.0



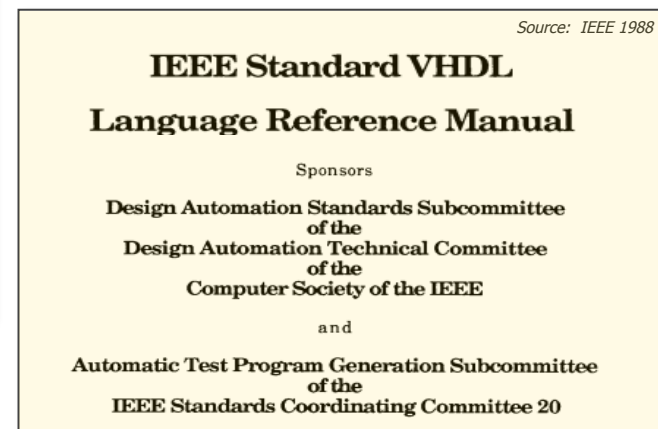
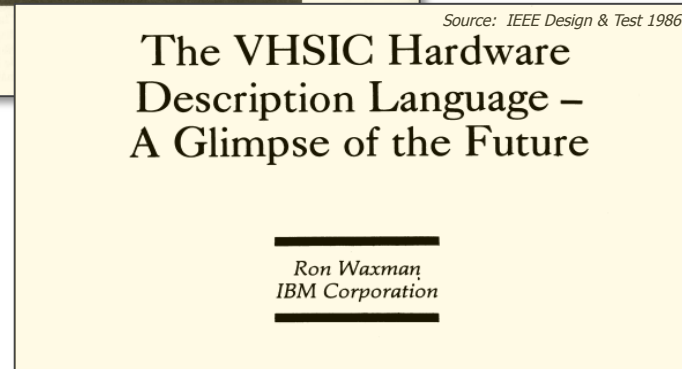
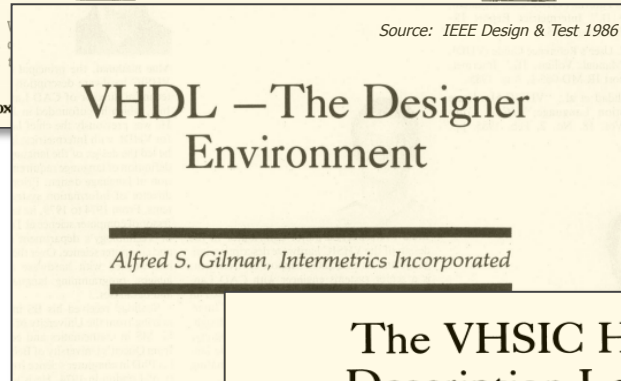
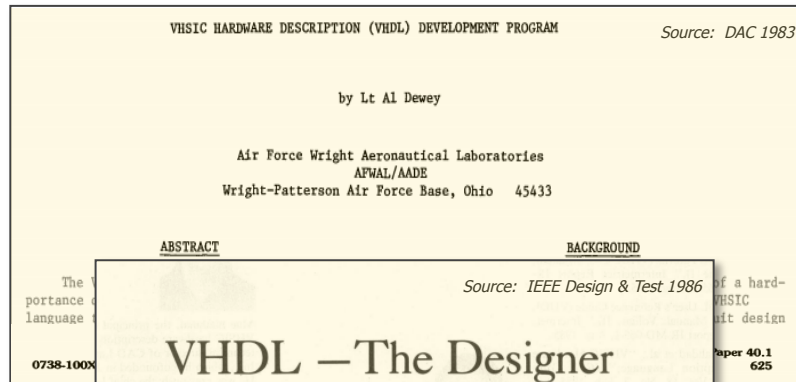
RTL ERA

Focus on Languages and
Improving Performance



VHDL Hardware Description Language

- IBM, Texas Instruments & Intermetrics awarded contract – 1983
 - VHSIC Hardware Description Language
 - VHDL 7.2 released in 1985
 - VHDL became IEEE Standard 1076 in 1987



Verilog Hardware Description Language



**ZZZip Through VLSI Design
With VERILOG**

More than ever before VLSI designers need a single CAD system that provides accurate, high-speed simulation of complex designs traversing all design levels - architectural, microcode, behavioral, RTL, gate, and switch. VERILOG takes you through all levels with a single homogeneous language.

The powerful and interactive symbolic debugger permits you to home in on design errors and even override them without terminating your mixed-level simulation. VERILOG's high speed compilation lets you build models in seconds and roll into simulation. It's a unique interactive tool for both design and simulation.

Get on the Fast Track

VERILOG handles even complex descriptions at speeds markedly faster than comparable systems. Simulating an 8085 microcomputer on a small 68010-based workstation, VERILOG barrels along at seven instructions per second - after building the model in six seconds flat. Gate and switch level simulation speeds rival those of gate-level only simulators.

With Interactive Control

Because VERILOG is interactive, testing and revising a design is efficient and flexible. A sophisticated symbolic debug with highly selective source trace tells you what is being simulated along with results. You can pinpoint problem areas quickly, update the design, and return to simulation in record time - a truly interactive process. Convenient batch-mode processing provides maximum flexibility.

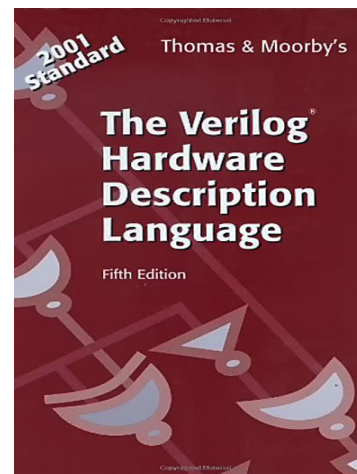
Ride the Right Track

A single homogeneous language at all levels for design description, waveform description, expected responses, symbolic debug, and interaction - all in VERILOG. You can link most software programs with your hardware description in VERILOG and simulate your software with your hardware design. A large SSI/MSI model library facilitates PCB design. VERILOG runs on a host of machines - Apollo, Sun, DEC/VAX, UNIX machines, and soon, IBM.

Fast, flexible, and functional, VERILOG lets you coast to successful logic design.

**GATEWAY
DESIGN AUTOMATION CORPORATION**
P.O. Box 1546, 235 Great Road, Littleton, MA 01460 (617) 486-9701

- Gateway Design Automation – 1985
 - Verilog HDL created by Phil Moorby in 1984
 - Acquired by Cadence in 1989
 - Verilog became IEEE Standard 1364 in 1995

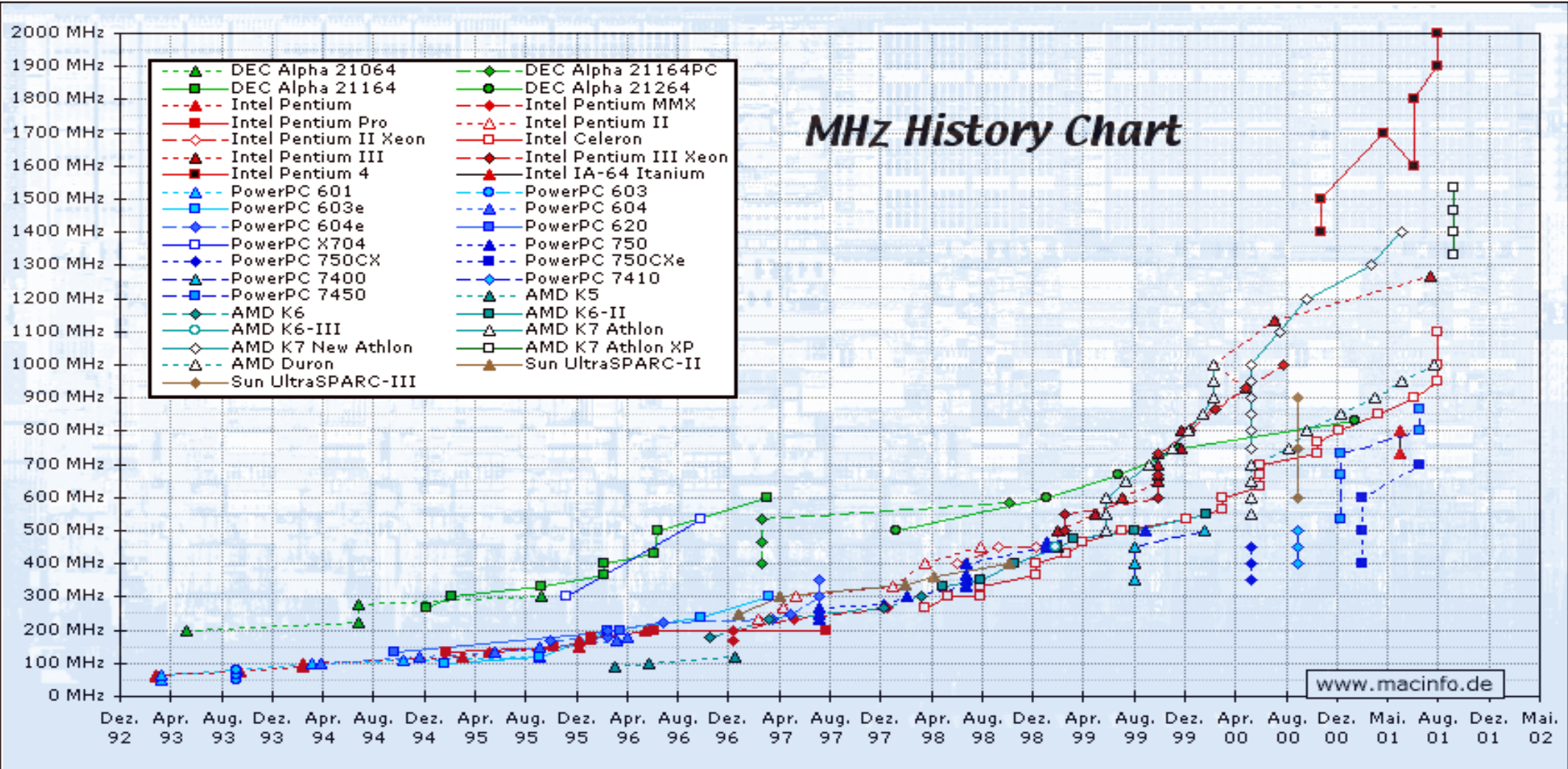


Source: IEEE Design & Test of Computers, August 1985

Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

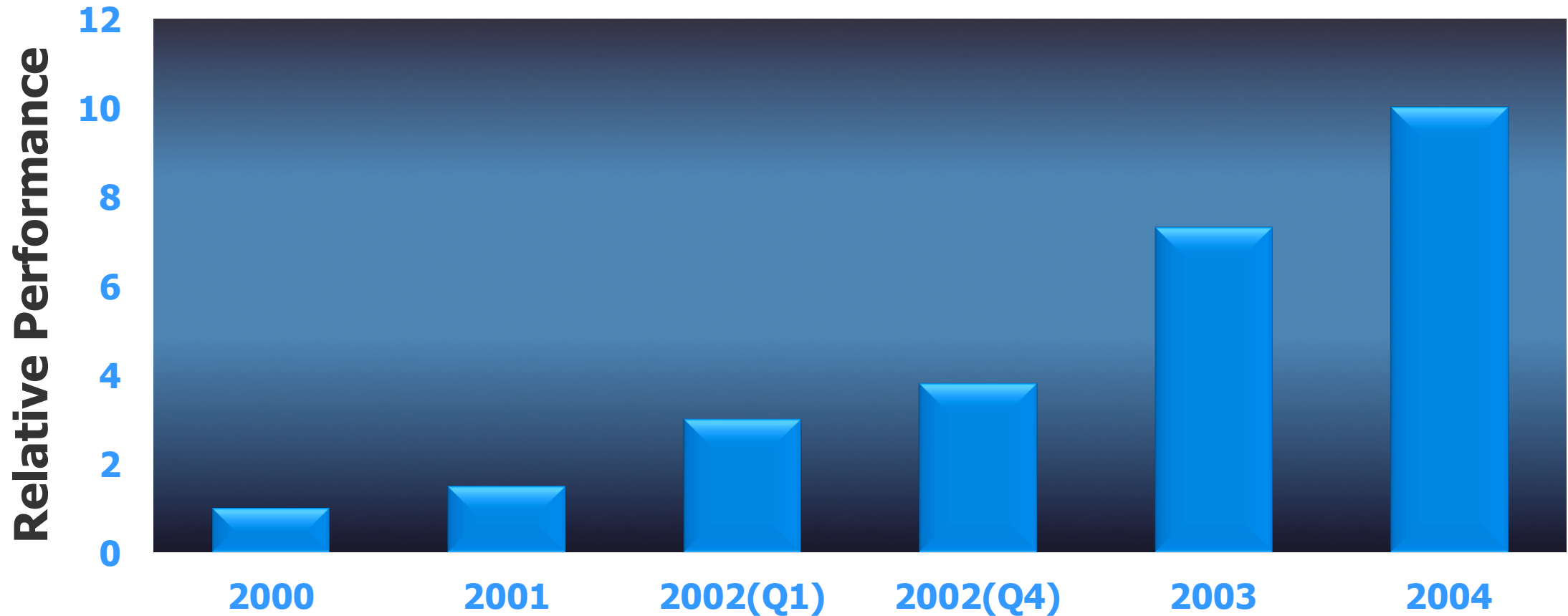
Ever-Improving Compute Performance



Source: www.macinfo.de

RTL Simulation Accelerates Independent of Hardware Performance

VERIFICATION 1.0



Source: Mentor Graphics

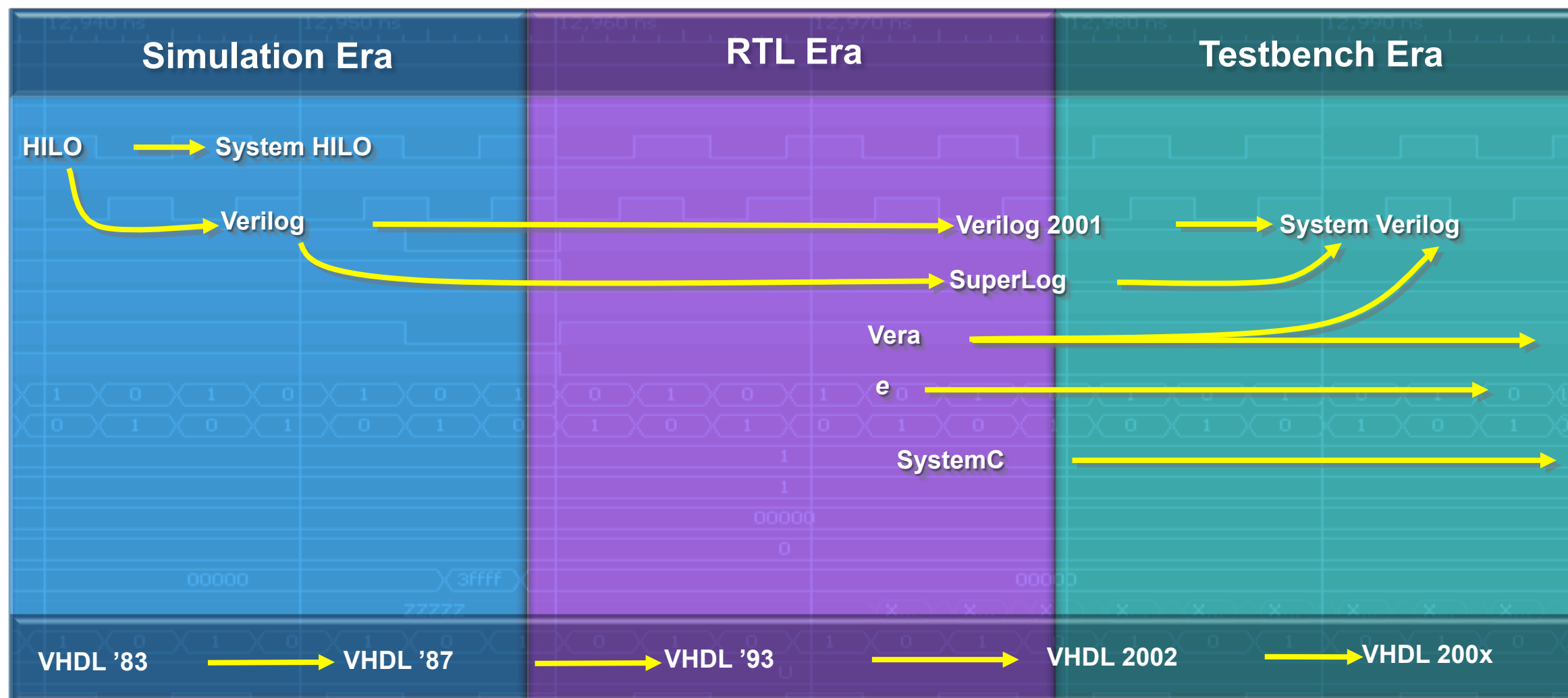
Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

Verification 2.0

TESTBENCH AUTOMATION FOCUS ON METHODOLOGIES

Language Evolution



Industry Converges on IEEE 1800



IEEE unifies Verilog standards efforts

Richard Goering

6/24/2004 3:00 PM EDT

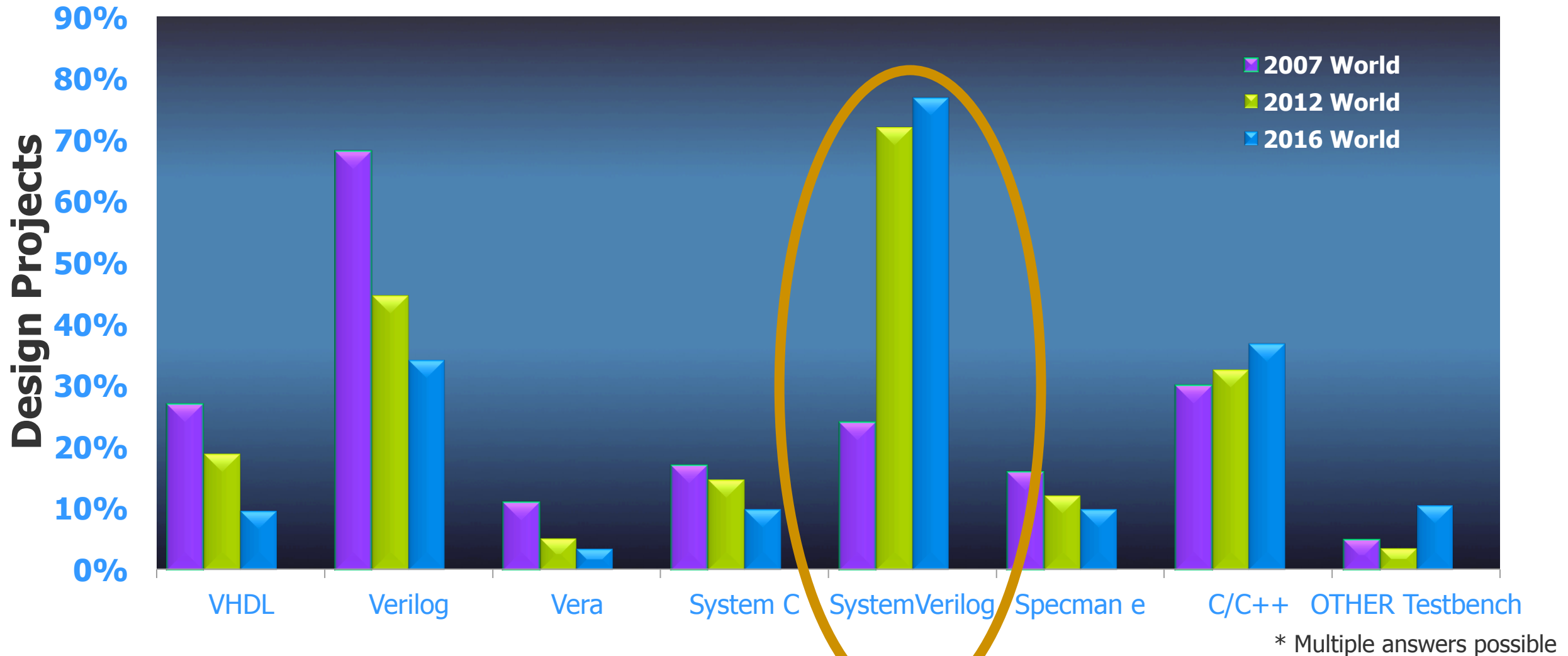
SANTA CRUZ, Calif. — Putting to rest fears of a Verilog language schism, the IEEE has decided to form a single working group that will encompass both SystemVerilog and the further evolution of the IEEE 1364 Verilog language standard.

The move follows criticisms of Accellera's decision to take SystemVerilog to a new IEEE working group rather than the existing 1364 committee.

In May, Accellera voted to take SystemVerilog to a new working group under the

SystemVerilog Becomes Mainstream Verification Language

VERIFICATION 2.0

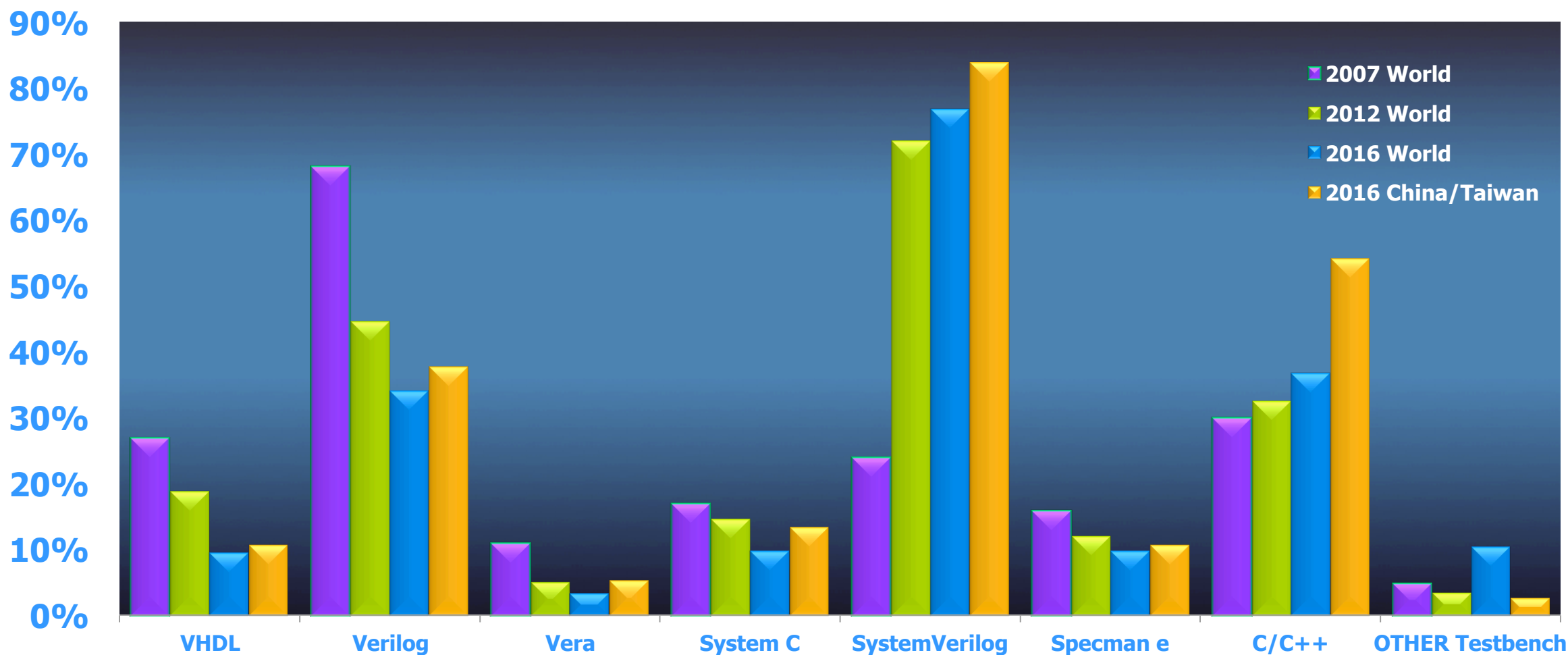


Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study - Excludes FPGA Devices

Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

China/Taiwan a Leader in SystemVerilog Adoption



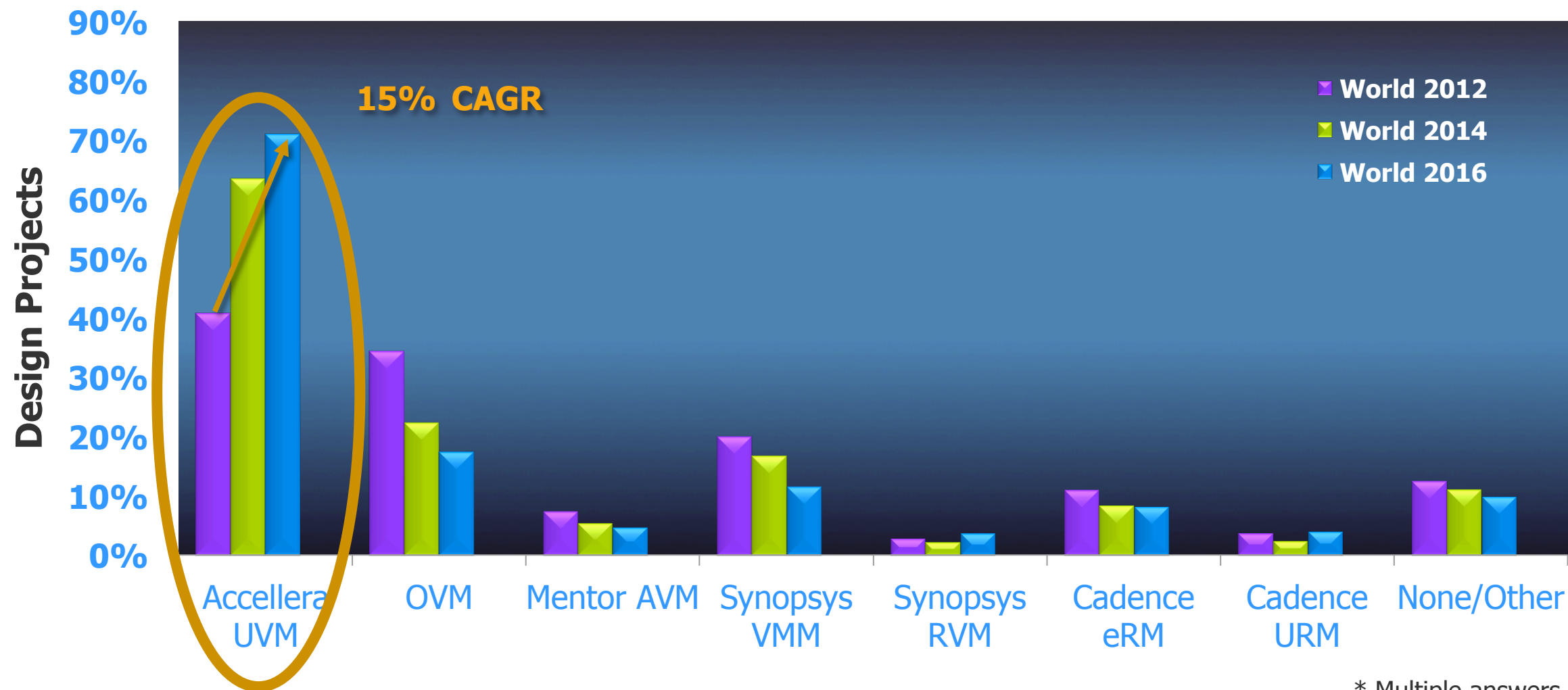
* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study - Excludes FPGA Devices

Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

Class Library Standardization Around UVM



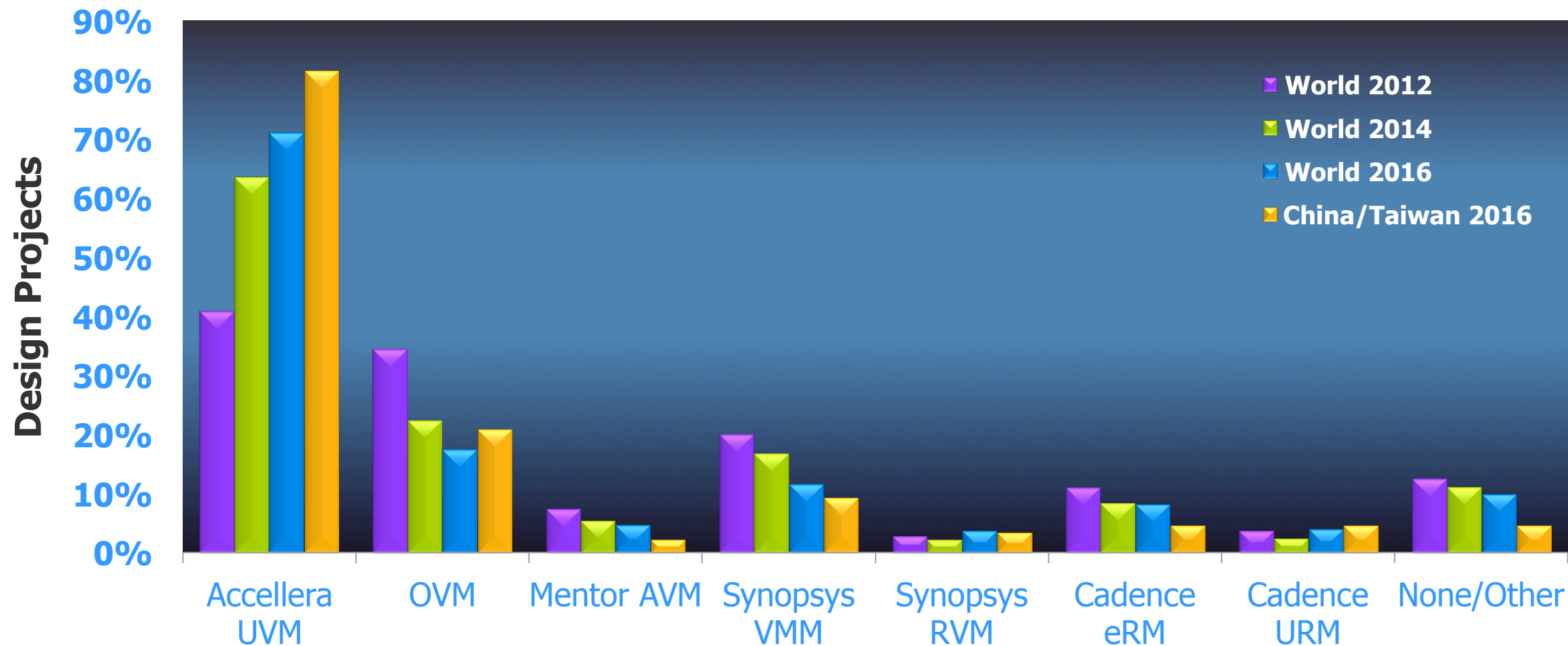
* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study - Excludes FPGA Devices

Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

China/Taiwan a Leader in UVM Adoption



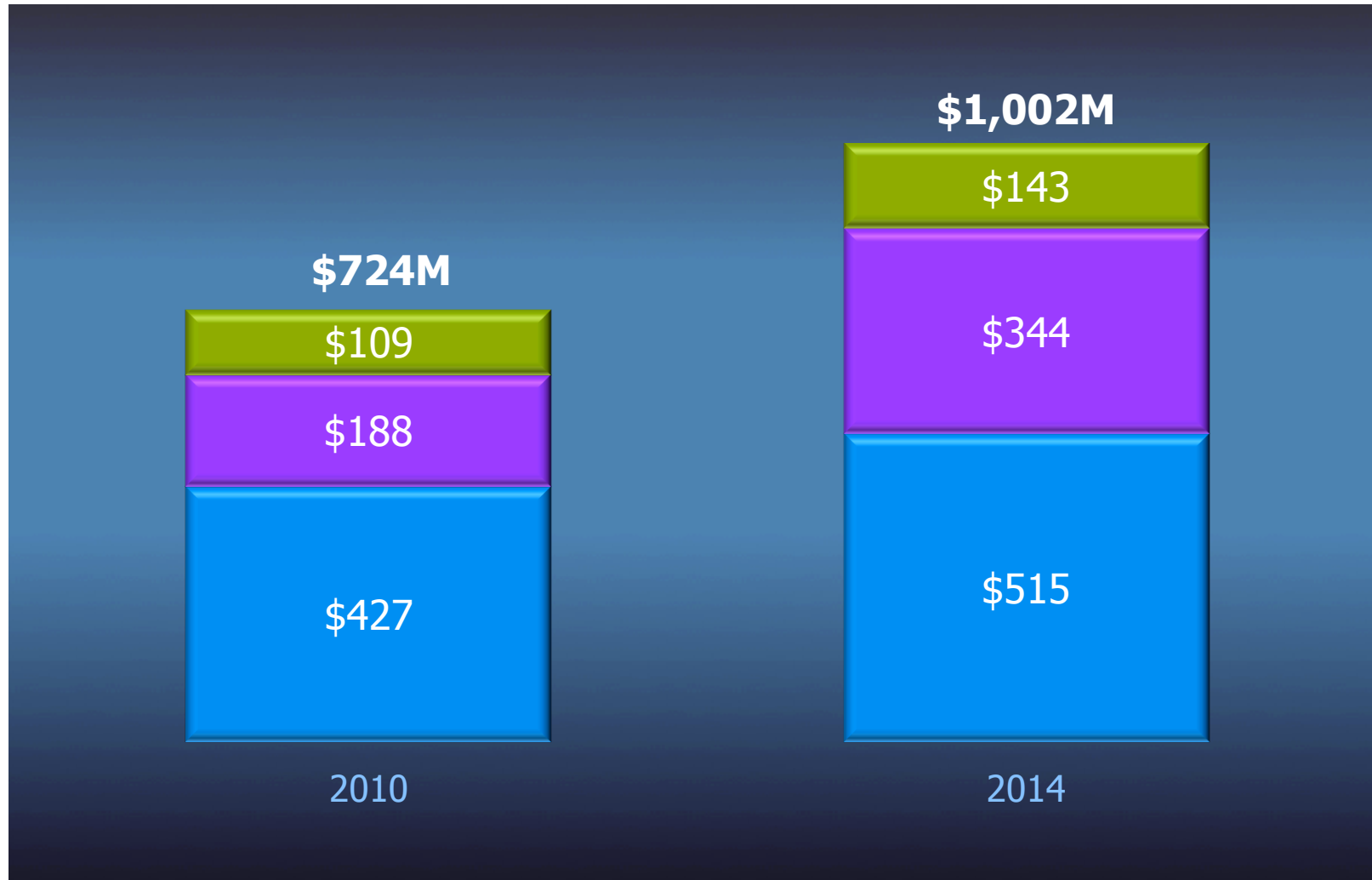
* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study - Excludes FPGA Devices

Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

Verification Is a \$1 Billion Market



2010-2014 CAGR
Total 9%

Formal 7%

Emulation 16%

Simulation* 5%

*Includes dynamic RTL simulation tools
Source: EDAC Market Statistics Service

The background is a high-resolution, blue-tinted photograph of a complex printed circuit board (PCB). The board is densely packed with intricate circuitry, including numerous microchips, resistors, and a complex network of fine copper traces. The overall aesthetic is technical and futuristic. Overlaid on this background are two main text elements: 'VERIFICATION 3.0' at the top and 'SYSTEM ERA' in the center. There are also some smaller, less legible markings on the board itself, such as 'NSTE LMC6442A' on the left and '1996' at the bottom left.

VERIFICATION 3.0

SYSTEM ERA

Integrating Cross-Domain Systems: An Automotive Example

Software

**Market
Drivers**

Hardware Complexity

High Cost of Failure



IVI



Driver Information



ADAS



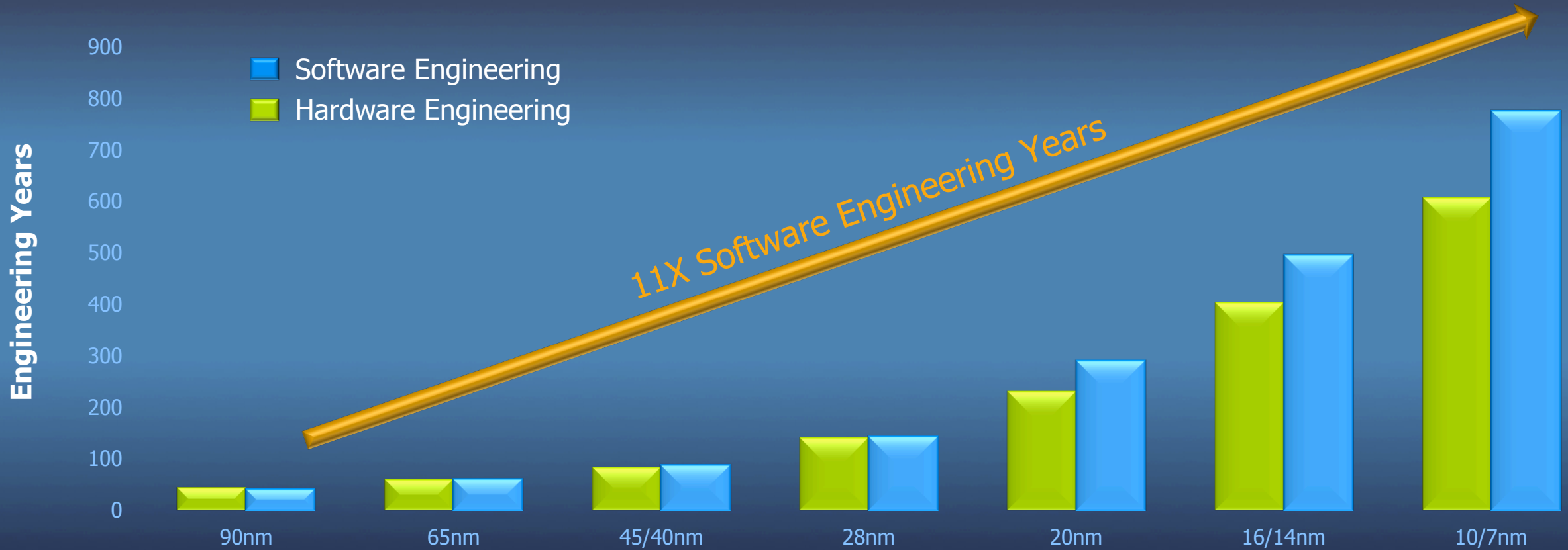
Telematics



Car Network

- Integrating cross-domain systems exposes emergent behavior earlier in the design process; Functional, Performance, Safety/Security, Connectivity

Embedded Software Development Headcount Surges past Hardware Design and Verification Headcount



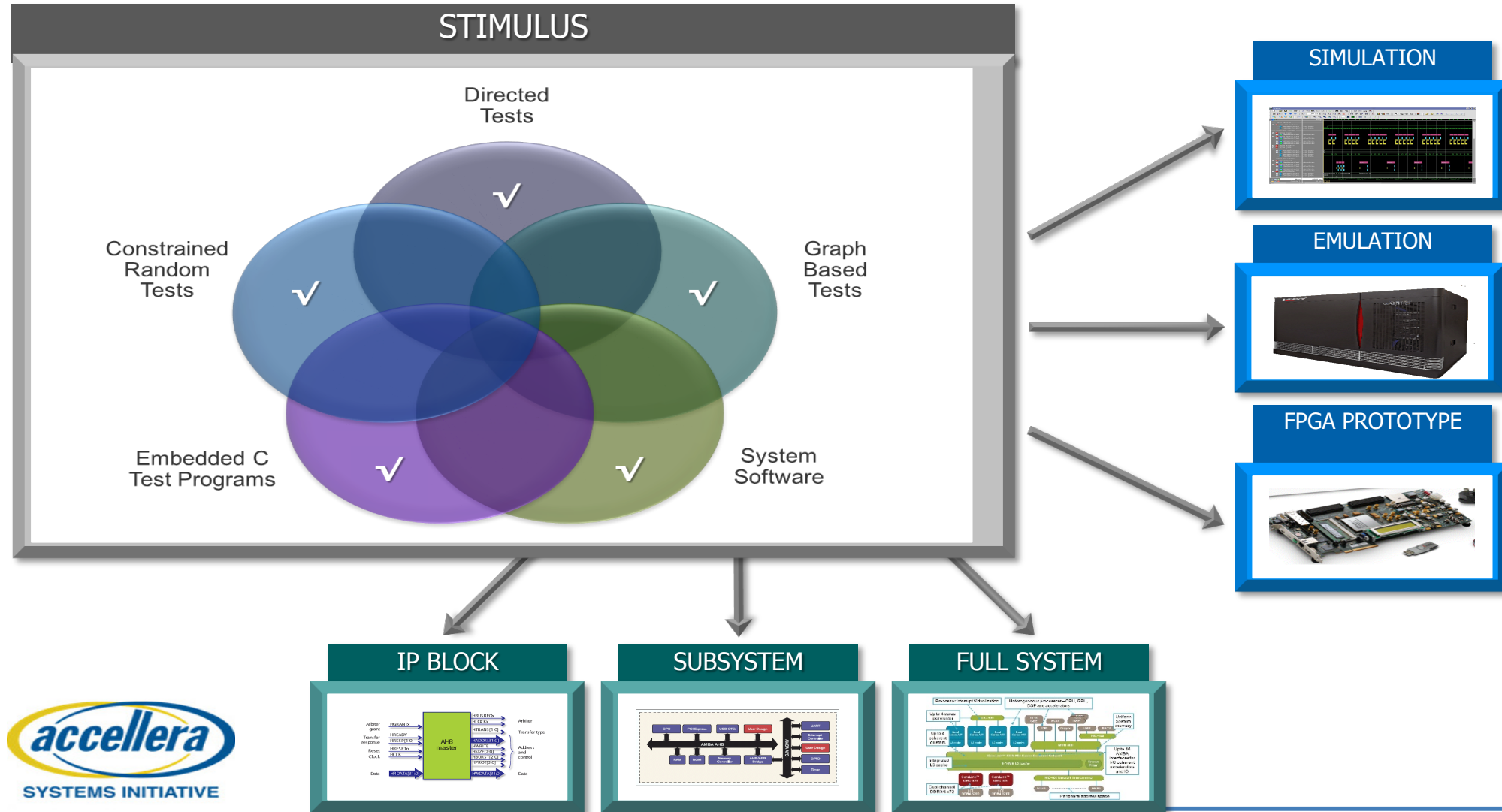
Source: International Business Strategies, Inc. (IBS), 2015

Restricted © 2017 Mentor Graphics Corporation

Mentor
A Siemens Business

**WHAT'S NEXT
FOR SYSTEM ERA?**

Improved Stimulus Generation with Portable Stimulus

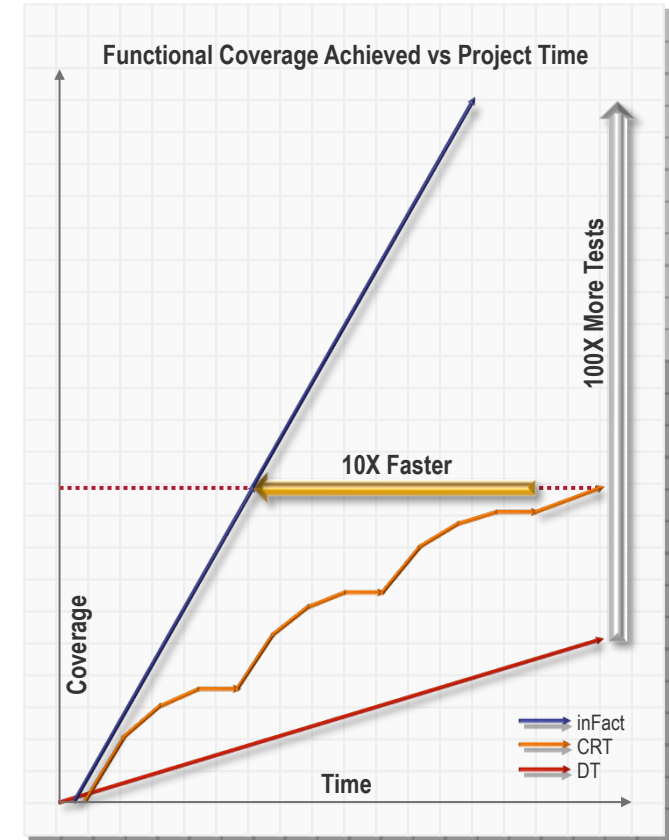


Restricted © 2017 Mentor Graphics Corporation

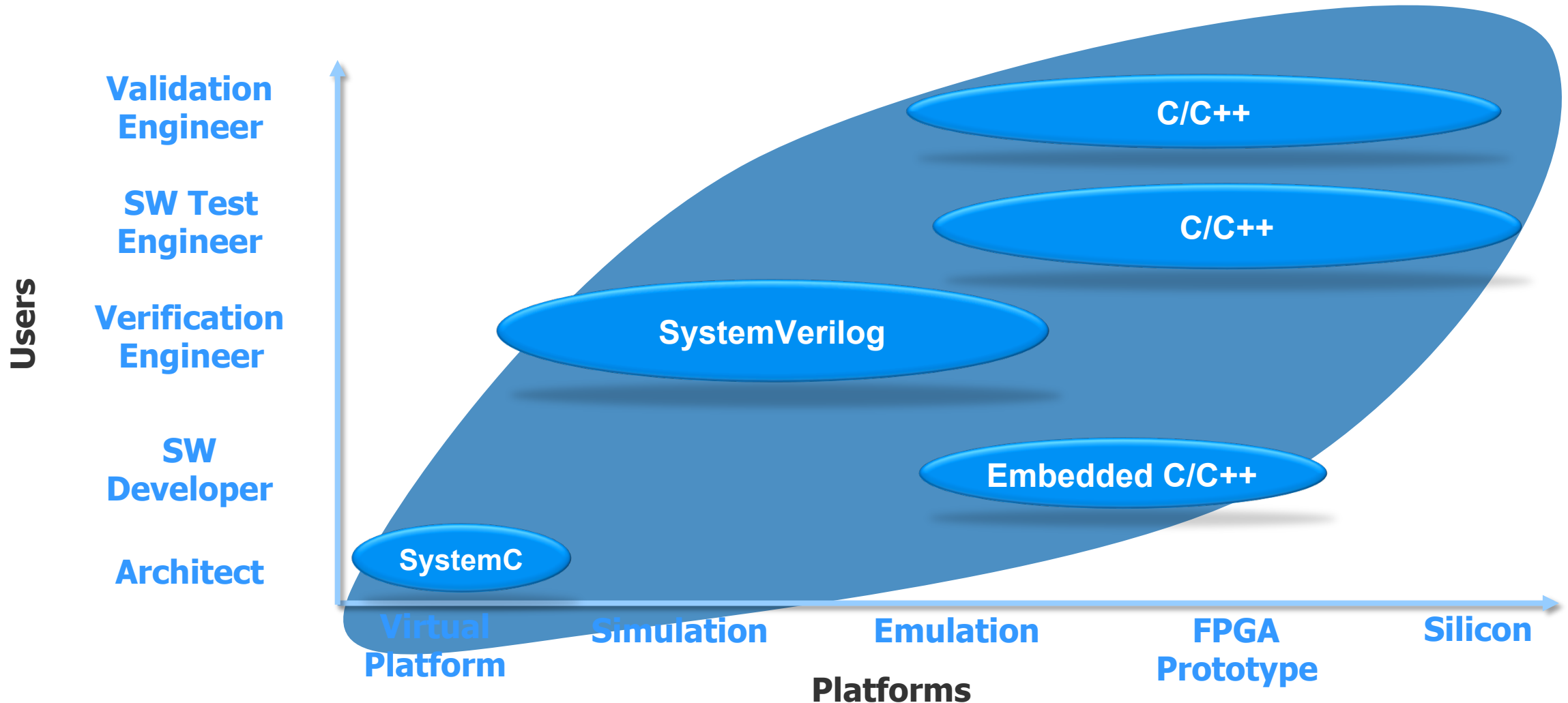
Mentor
A Siemens Business

Supporting Portable Stimulus Technology

- Accelerates Coverage Closure
 - No wasted stimulus
 - 10-100x faster ramp to coverage goals
 - Fewer simulation resources
- Expands Directed Tests
 - Re-use existing stimulus description
 - Generate even more tests
 - Boosts verification comprehensiveness
- Integrates Easily
 - Flexible testbench environment support
 - Non-invasive integration
 - Reuse existing BFM/checkers

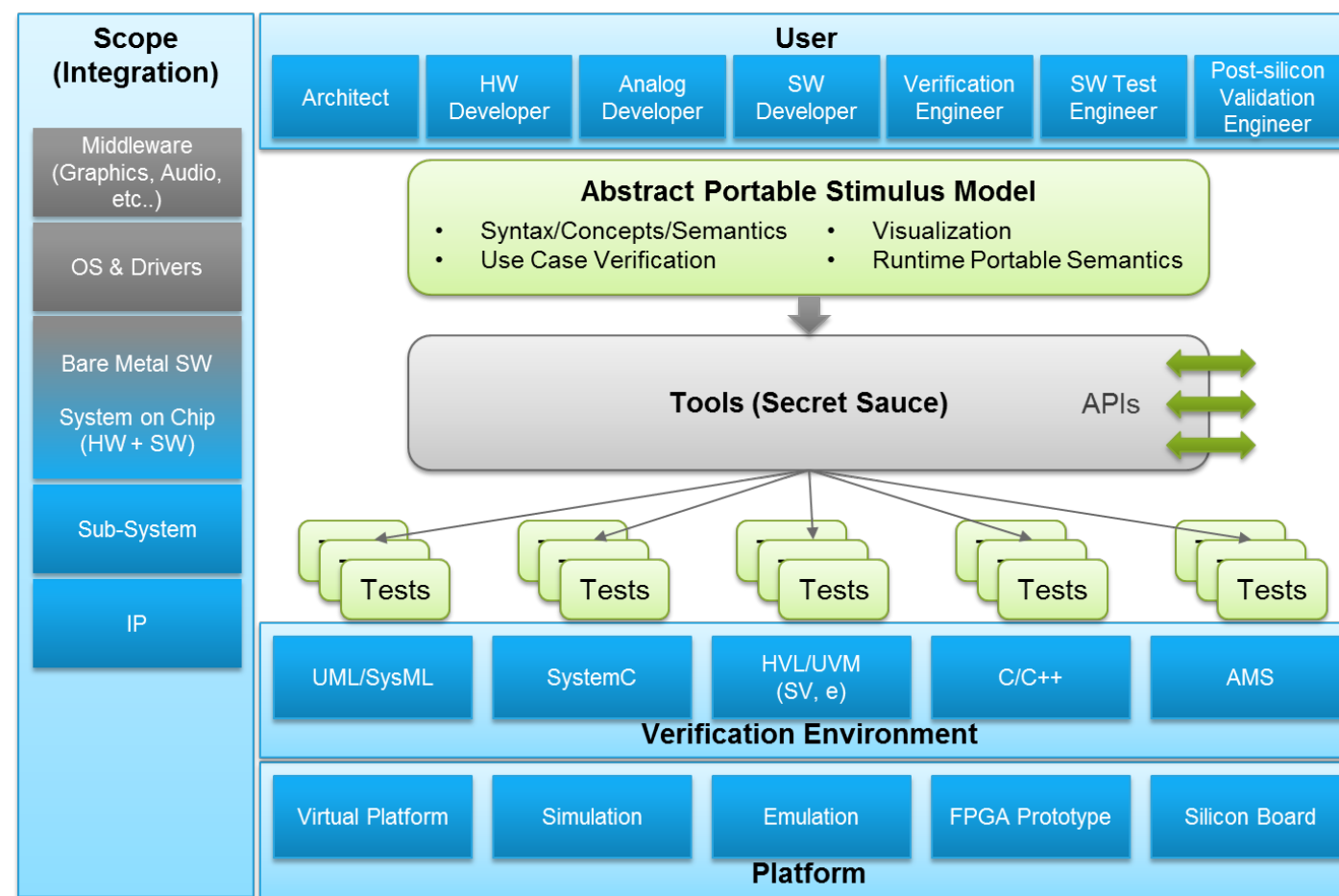


Evolution of the Portable Test Bench

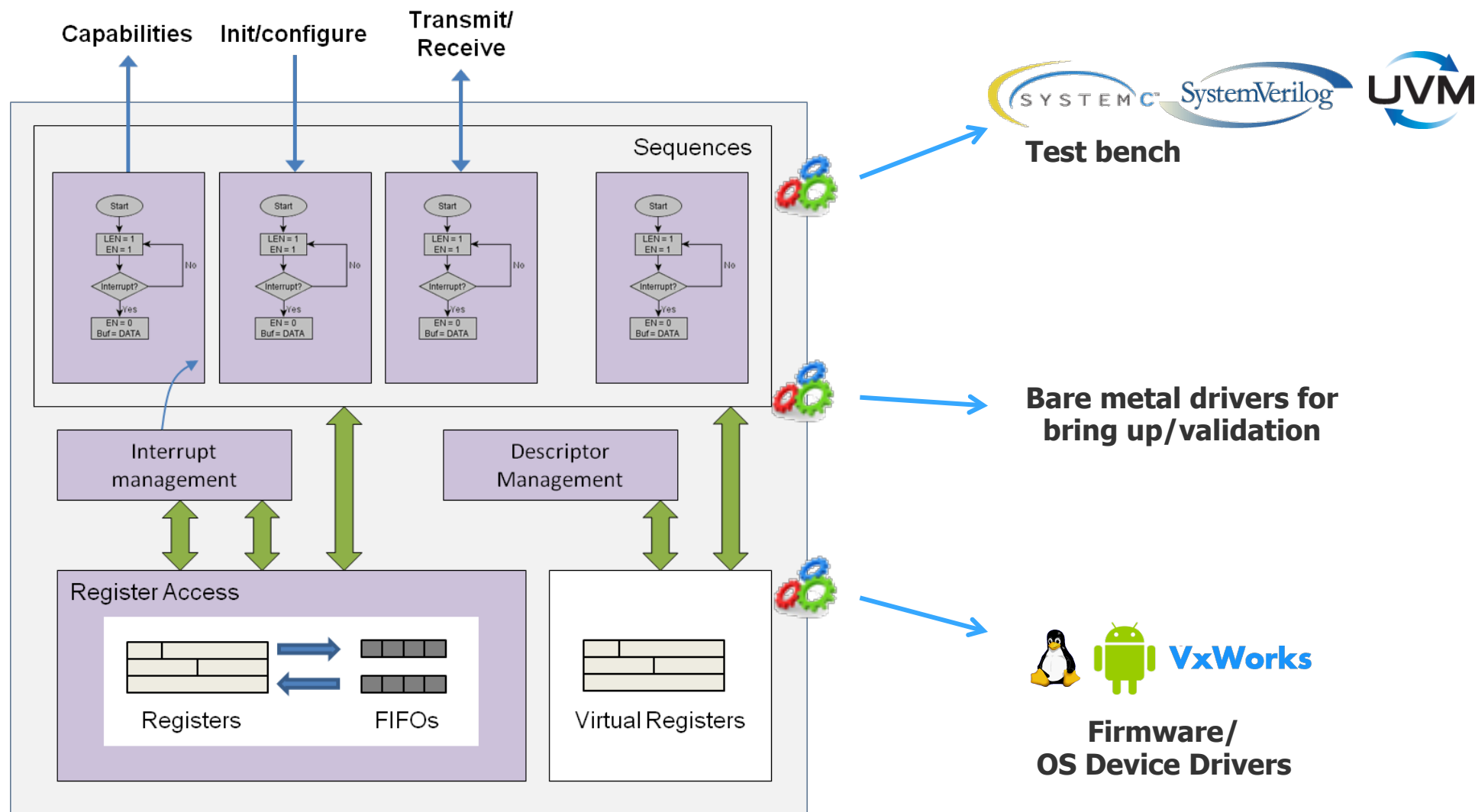


Portable Stimulus Working Group

- Single input specification
- Enable test creation automation
- Reusable across all platforms
- Tools generate specifics

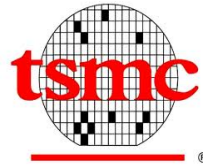


Truly Portable Stimulus Emerging



Portable Stimulus Example

■ TSMC Collaboration Addresses Improved Pattern Generation



- "Design verification complexity is a major barrier to reach coverage closure. Reducing overall design cycle time is a common goal for the semiconductor industry," said Suk Lee, director of Design Infrastructure Marketing at TSMC. "Our collaboration with Mentor Graphics on Questa Ultra verification platform is an important step to address the time-to-coverage challenges that customers are facing today especially in pattern generation."

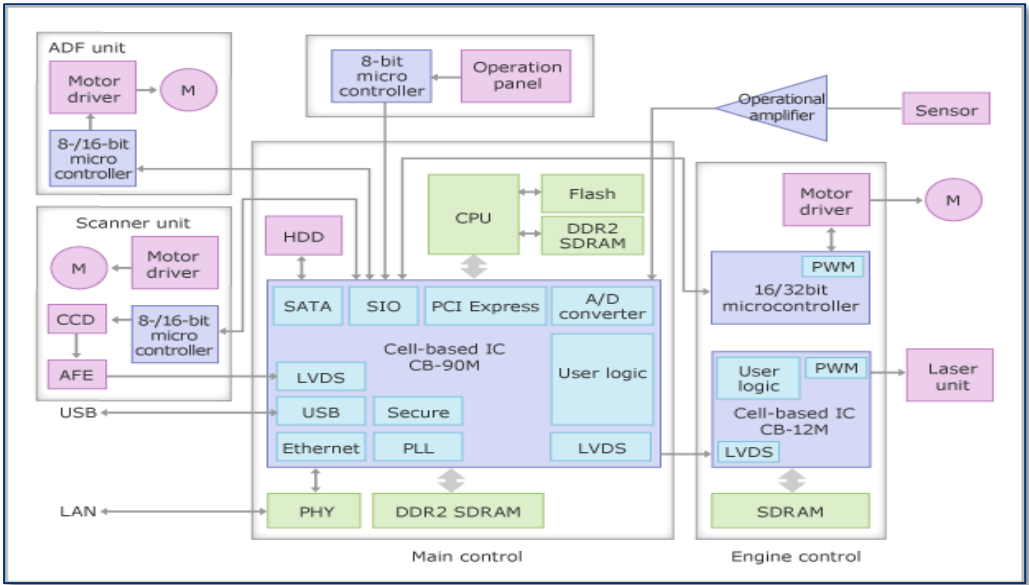
■ AppliedMicro Sees Dramatic Time-to-Coverage Improvements



- "AppliedMicro always evaluates tools that make tough design verification challenges easier. The Mentor Graphics collaboration with TSMC results in verification technology that is user friendly and draws on a comprehensive tool set in a standard methodology framework," said Shing Sheung Tse, senior engineering manager at AppliedMicro. "The technology offers the ability to employ advanced techniques and to manage overall coverage metrics for low-power design verification. The Intelligent Testbench Automation capability shortens our time-to-coverage by over 100x. This feature-rich solution helps design teams consolidate tasks, reduce time-to-market and introduce advanced embedded processing for high-speed transport products."

Mentor Portable Stimulus Example

Industry	Office Products
Design	Printer Image Processor
Existing	Questa SystemVerilog CRT
New	Questa Ultra iTBA
Value 1	37 X Faster TTC
Value 2	+40% Coverage
Integration	1½ Day

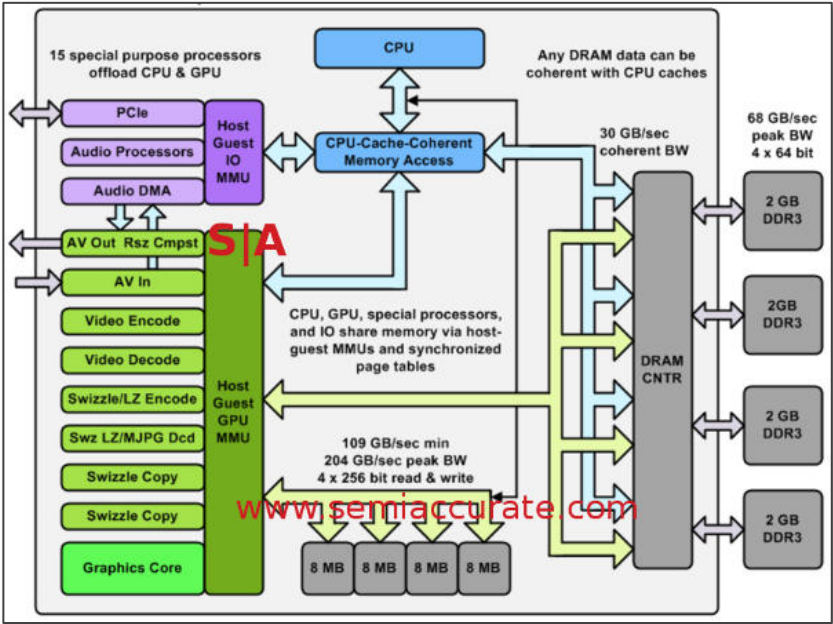


Multi-CPU testbench distribution reduced 8 week problem to a 1½ day solution

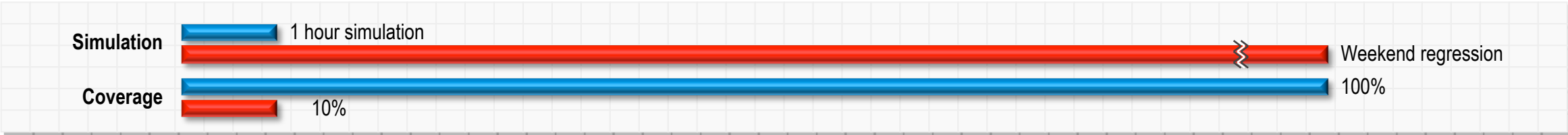


Mentor Portable Stimulus Example

Industry	Server on Chip
Design	Cache Controller
Existing	Questa SystemVerilog CRT
New	Questa Ultra iTBA
Value 1	+90% coverage
Value 2	No need to write directed tests
Integration	1/2 Day

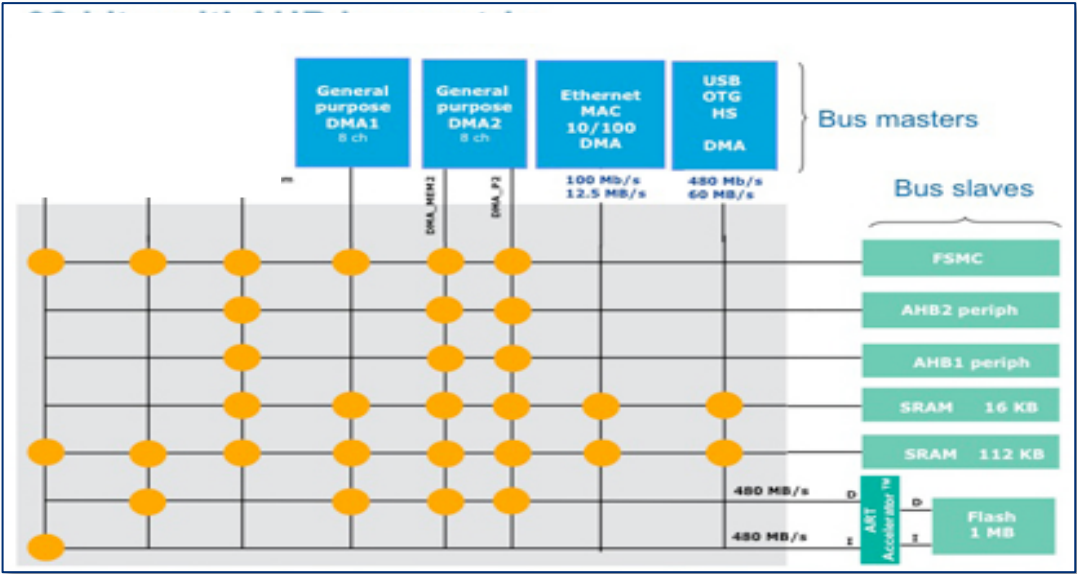


Complex coverage efficiently hit. No need to write directed tests

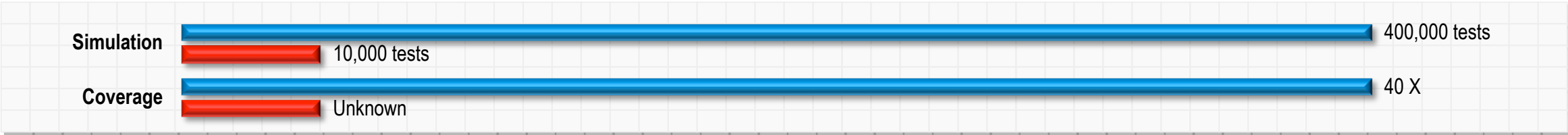


Mentor Portable Stimulus Example

Industry	Switching Systems
Design	Multi-Master Bus Fabric
Existing	Questa with directed random tests
New	Questa Ultra inFact
Value 1	40 X More Tests
Value 2	40 X Higher Coverage
Integration	2 Days



Expanded months worth of tests by 40 X in just 2 days. Used inFact to measure coverage.

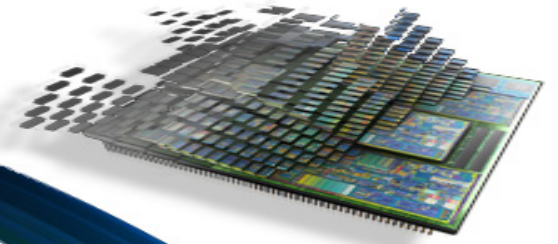


Accellera Portable Stimulus Webinar Series

- Part 1: Monday, April 10 at 8:00am PT
 - Discussion of verification productivity
 - Reasons the Portable Stimulus Standard was undertaken
 - Concepts and language constructs
- Part 2: Monday, April 17 at 8:00am PT
 - Block-level stimulus and verification intent models
 - System-level scenarios
 - Generate a test implementation on multiple platforms
- Part 3: Monday, April 24 at 8:00am PT
 - Model coverage
 - Hardware/software interface layer
 - Summary of standardization efforts and upcoming goals.
- Register: Visit <http://www.accellera.org/news/events>

Verification Academy

The most comprehensive
resource for verification training



<https://verificationacademy.com/courses/portable-stimulus-basics>

- Comprehensive on-line training
 - Self-paced training
 - More than 22,000 members
 - New Portable Stimulus course
- World-wide forum discussions
 - 4400+topics
- Verification Methodology
 - Coverage Cookbook
 - UVM Cookbook

Portable Stimulus Basics



****NEW COURSE****

The new Portable Stimulus Standard being worked on in Accellera promises to provide the next leap in verification productivity needed to support the verification of our ever-growing system-on-chip (SoC) designs. In addition to increased complexity, SoC verification requires multiple platforms, including simulation, emulation and

FPGA prototyping, each of which typically use different languages and formats for specifying the test, wasting precious time recreating the same test information throughout a project. Portable Stimulus attempts to address this problem by providing a single specification of test intent and coverage at a higher level of abstraction, allowing tools to generate target-specific implementations of the test for the desired platforms and freeing up the verification team to focus on what should be tested. In addition, Portable Stimulus also raises the level at which randomization can be applied, allowing many different but compatible scenarios to be generated from a single graph-based specification of test intent.

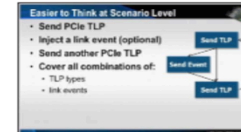
This Verification Academy course will provide an introduction to the upcoming Portable Stimulus standard, starting with a discussion of the need for and goals of the standard, taking the viewer through the actual standard itself to provide an understanding of how to create your own specification of Portable Stimulus and how a tool can generate UVM, C or other implementations of the test for your required platform.

Tom Fitzpatrick Coverage Simulation-Based Techniques Walk

Sessions

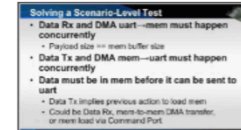
Why Portable Stimulus?

This session will discuss the motivation and goals for Portable Stimulus, explore the idea of scenario-level stimulus and examine the requirements for a viable Portable Stimulus solution.



What is Portable Stimulus?

This session will provide a detailed understanding of what a scenario-level test actually involves; how to think and plan at the scenario level; and how a single scenario-level specification can be used to create multiple test scenarios.



Upcoming Sessions

- Portable Stimulus Use Models
- Introducing the Accellera Portable Stimulus Standard
- Building System Level Scenarios with the Accellera Portable Stimulus Standard
- Generating Tests from Portable Stimulus

Summary

- Despite design re-use, verification complexity continues to increase at 3-4X the rate of design creation
- Increasing verification requirements drive new capabilities for each type of verification engine
- Continuing verification productivity gains require EDA to:
 - Abstract the verification process from the underlying engines
 - Develop common environments, methodologies and tools
 - Separate the “what” from the “how”
- Portable Stimulus promises another leap in verification productivity
 - Invest in yourself: Keep current with Portable Stimulus development

